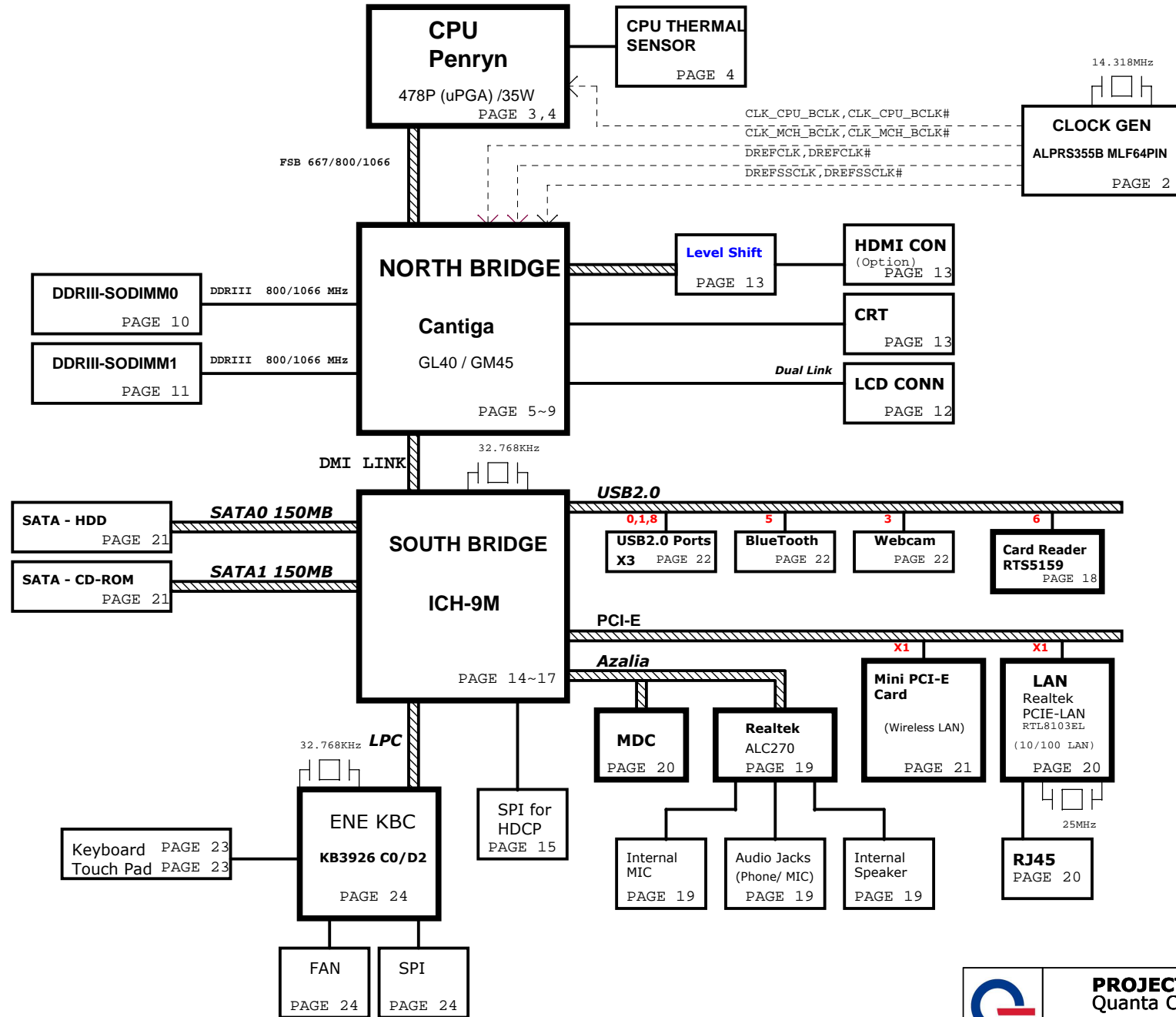


Wimbledon AX3/5 BLOCK DIAGRAM

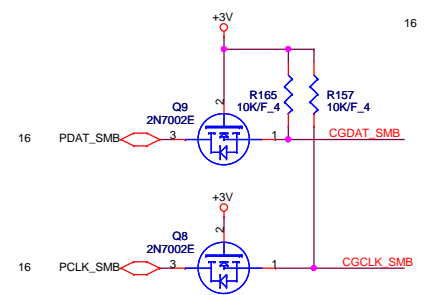
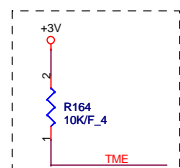
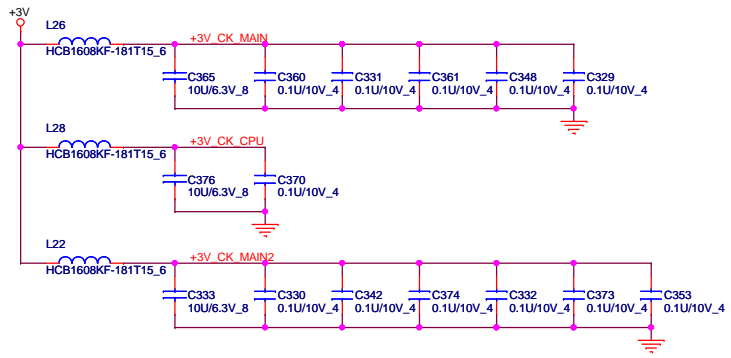
PCB STACK UP
6L UMA CO-LAY DIS

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



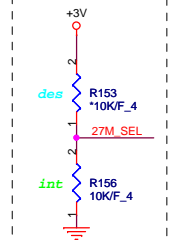
- SYSTEM CHARGER (ISL6251AHAZ-T) PAGE 25
- SYSTEM POWER (RT8206BGQW) PAGE 26
- VCCP +1.05V (RT8209AGQW) & +1.8VSUS (RT9043GB) PAGE 27
- CPU CORE (ISL6262ACRZ-T) PAGE 28
- DDR III SMD DR +1.5VSUS (RT8207AGQW) PAGE 29
- SYSTEM DISCHARGER PAGE 30

3,4,5,6,8,9,14,17,27,28 +1.05V
4,6,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V

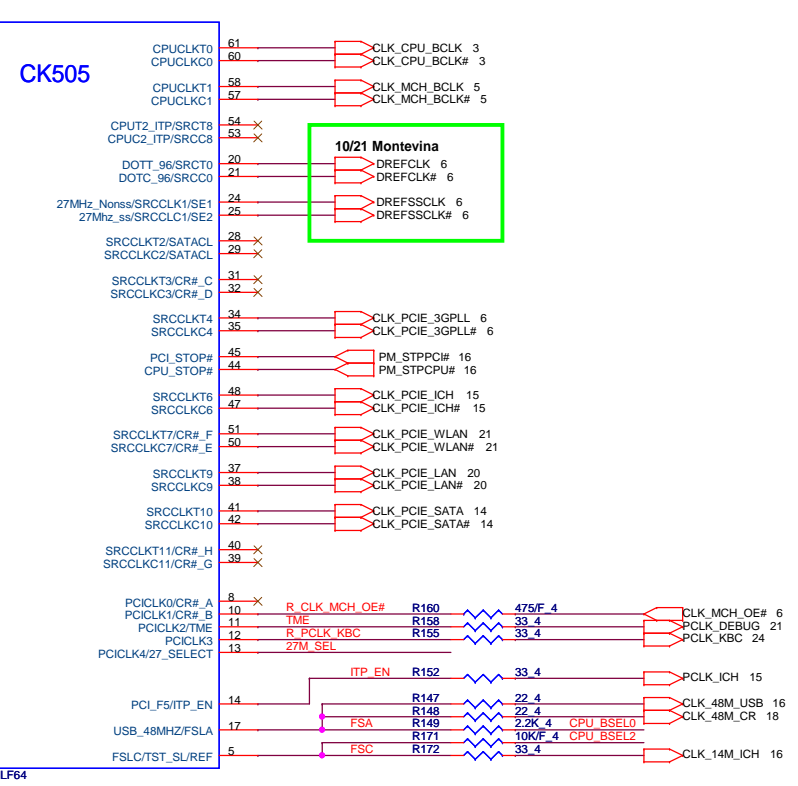
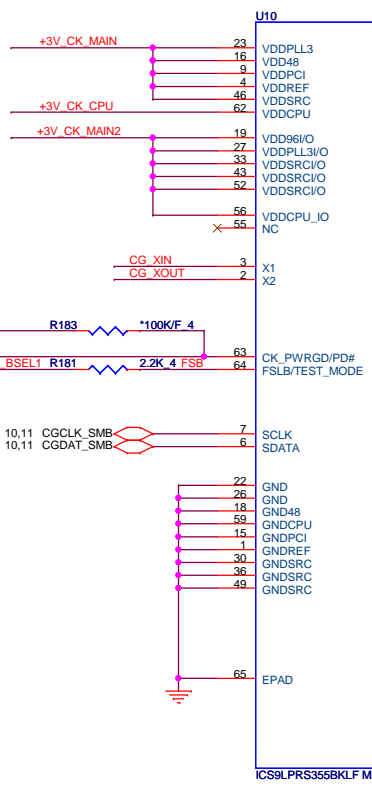
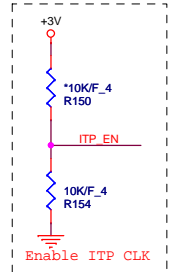


DB:Change from 27P to 33P(TXC suggestion)

0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



0=UMA
1 = External VGA

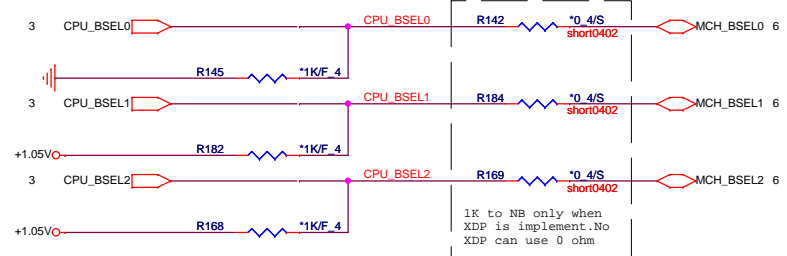


CK505 QFN64

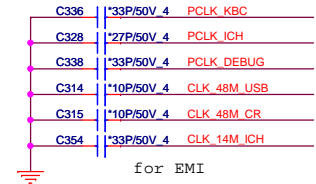
Silego SLG8SP513VTR AL8SP513000
Realtek RTM875N-606-VD-GR AL000875000
ICS ICS9LPRS355BKLF ALPRS355000

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CPU Clock select



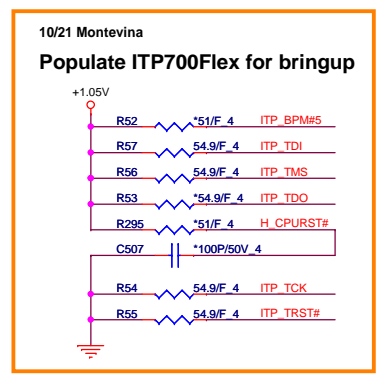
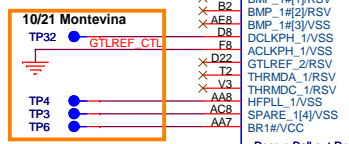
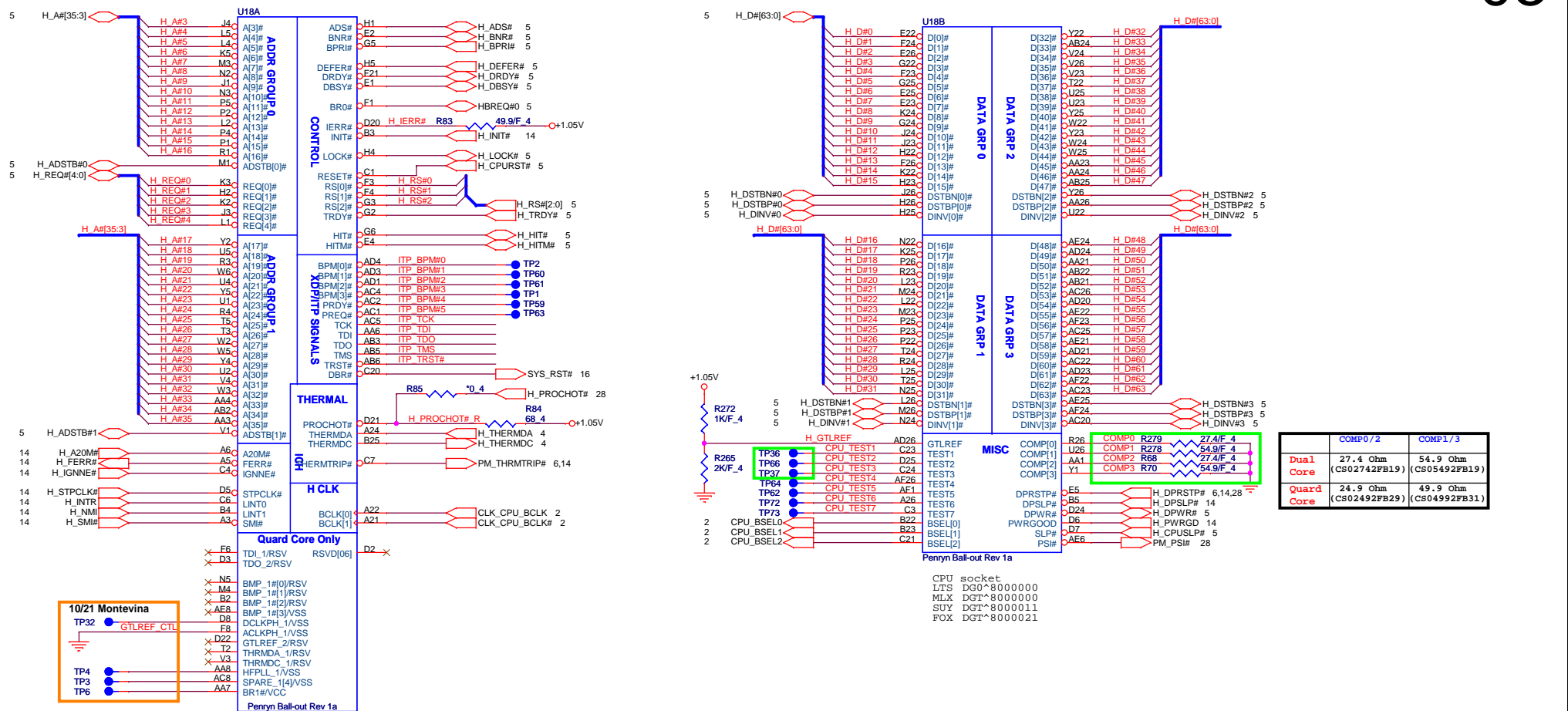
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



PROJECT :AX3
Quanta Computer Inc.

NBS5

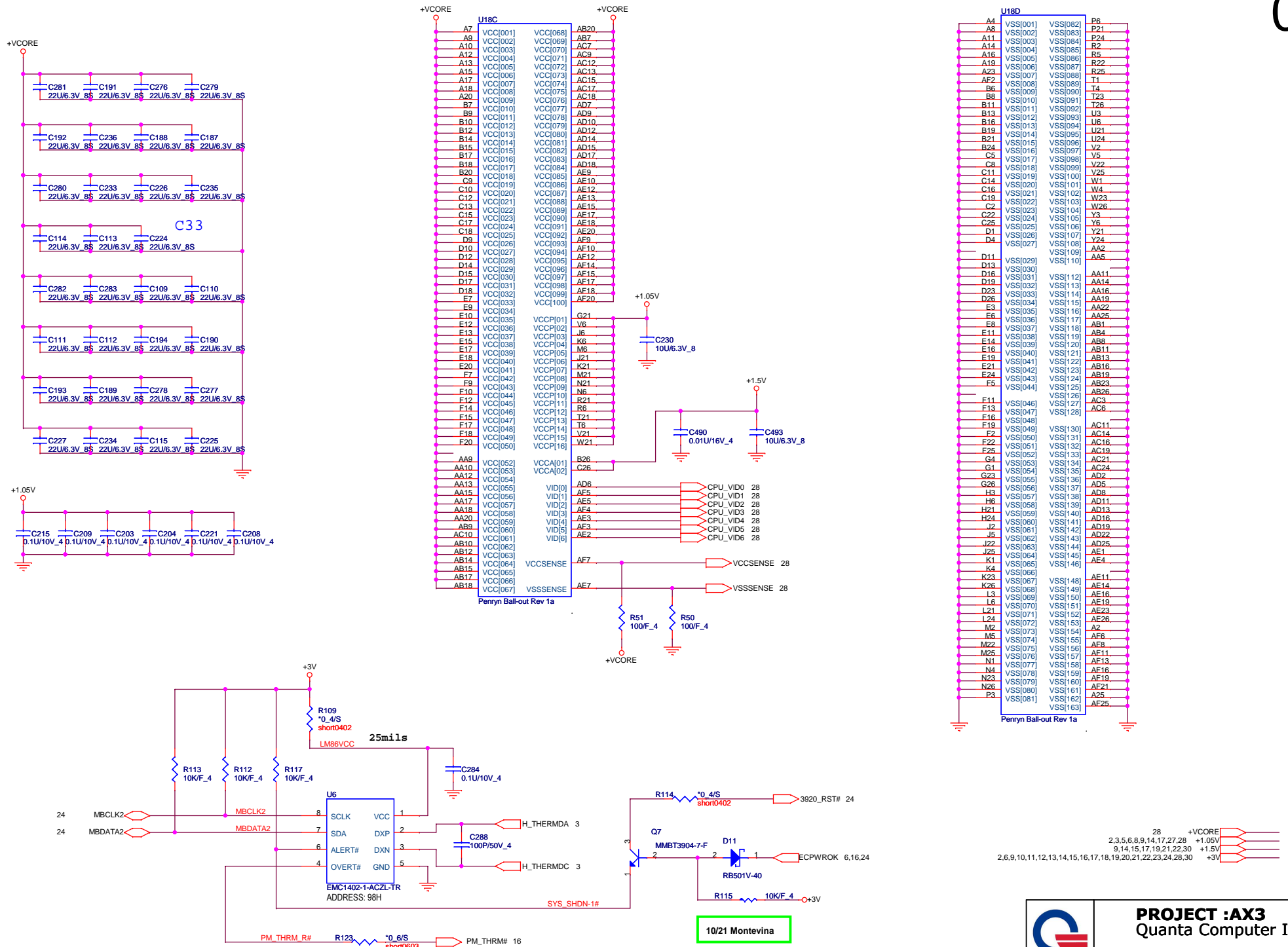
Size Custom Document Number **Clock Generator** Rev 1A
Date: Friday, November 27, 2009 Sheet 2 of 30



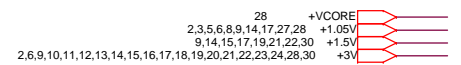
2,4,5,6,8,9,14,17,27,28 +1.05V

PROJECT :AX3
Quanta Computer Inc.

Size Custom	Document Number Penryn Host 1/2	Rev 1A
Date: Friday, November 27, 2009		Sheet 3 of 30



U18D	VSS[001]	VSS[082]	P6
A4	VSS[001]	VSS[082]	P21
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
AE2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T3
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B21	VSS[014]	VSS[095]	U24
B24	VSS[015]	VSS[096]	V2
B25	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C2	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D11	VSS[027]	VSS[108]	AA2
D13	VSS[029]	VSS[110]	AA5
D16	VSS[030]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB16
E21	VSS[042]	VSS[123]	AB19
E24	VSS[043]	VSS[124]	AB23
F5	VSS[044]	VSS[125]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[130]	AC11
F19	VSS[049]	VSS[131]	AC14
F2	VSS[050]	VSS[132]	AC16
F25	VSS[051]	VSS[133]	AC19
G4	VSS[052]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[148]	AE11
K23	VSS[067]	VSS[149]	AE14
K26	VSS[068]	VSS[150]	AE16
L3	VSS[069]	VSS[151]	AE19
L6	VSS[070]	VSS[152]	AE23
L21	VSS[071]	VSS[153]	AE26
L24	VSS[072]	VSS[154]	A2
M2	VSS[073]	VSS[155]	A2
M5	VSS[074]	VSS[156]	AF6
M22	VSS[075]	VSS[157]	AF8
M25	VSS[076]	VSS[158]	AF11
N1	VSS[077]	VSS[159]	AF13
N4	VSS[078]	VSS[160]	AF16
N23	VSS[079]	VSS[161]	AF19
N26	VSS[080]	VSS[162]	AF21
P3	VSS[081]	VSS[163]	A25
			AF25

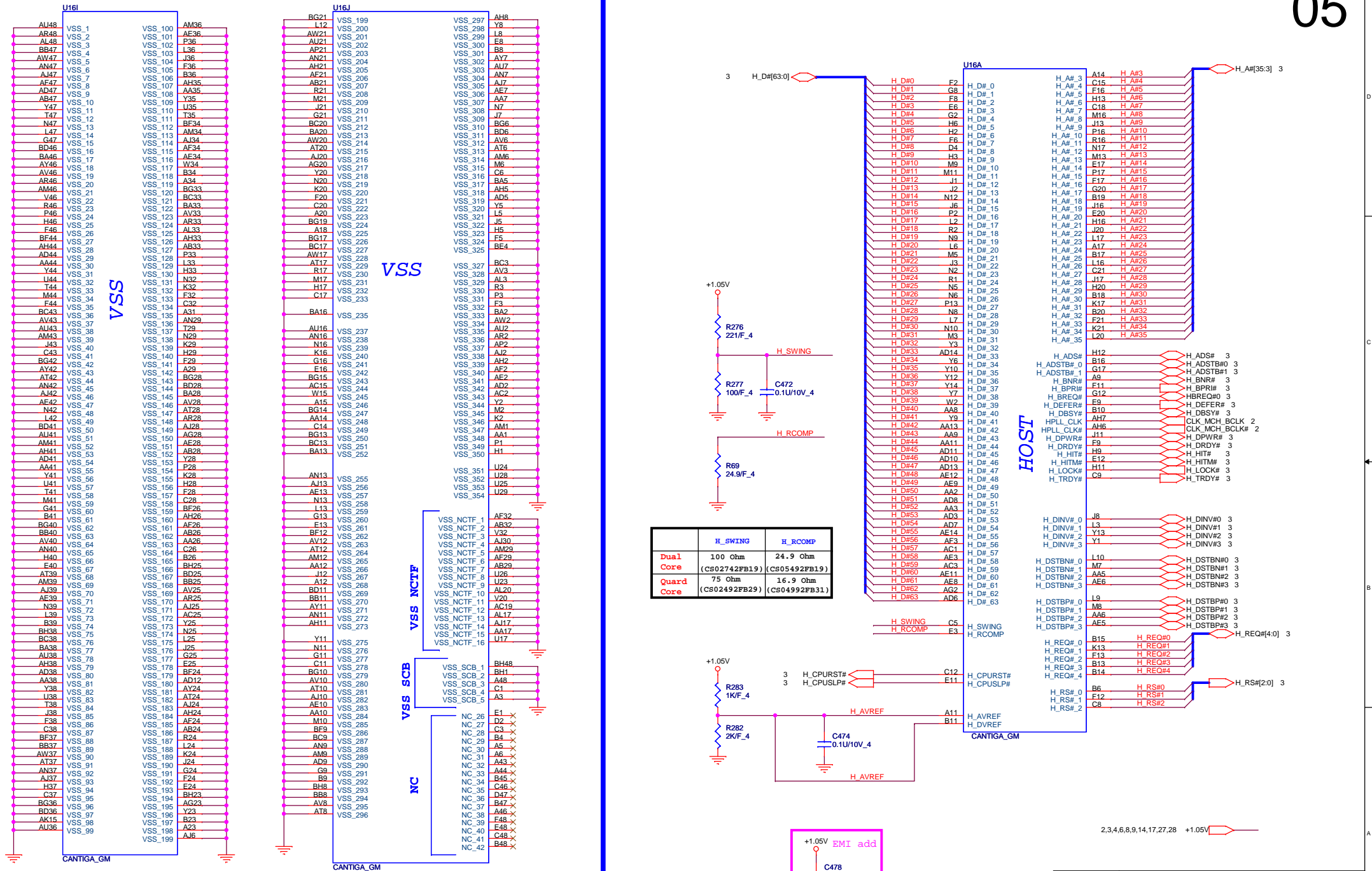


PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number Penryn & TH Monitor 2/2 Rev 1A

Date: Friday, November 27, 2009 Sheet 4 of 30

10/21 Montevina



	H_SWING	H_RCOMP
Dual Core	100 Ohm (C602742FB19)	24.9 Ohm (C605492FB19)
Quad Core	75 Ohm (C602492FB29)	16.9 Ohm (C604992FB31)

HOST

2,3,4,6,8,9,14,17,27,28 +1.05V

PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number **Cantiga Host & VSS 1/5** Rev 1A

Date: Friday, November 27, 2009 Sheet 5 of 30



MCH_CFG_5 DMix2 selection

Low: DMix2
 High: DMix4 (Default)
 MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
 High: Dynamic ODT enabled (Default)
 MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
 High: Normal operation (Default)
 MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
 High: Lane Reserved
 MCH_CFG_6 ITPM Host Interface

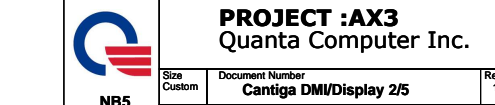
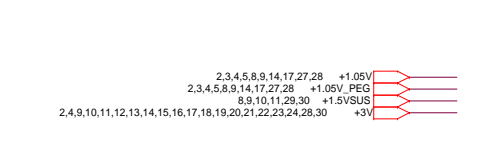
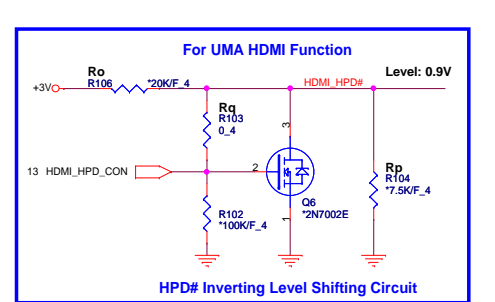
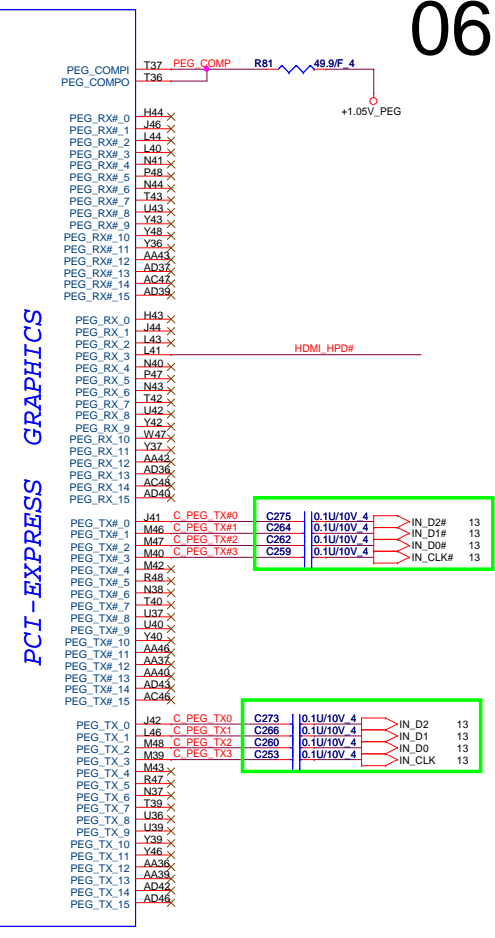
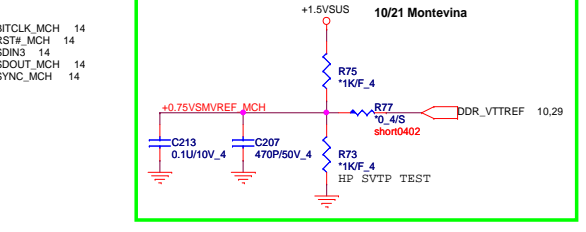
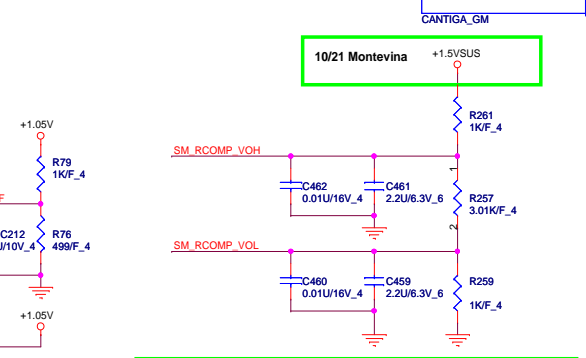
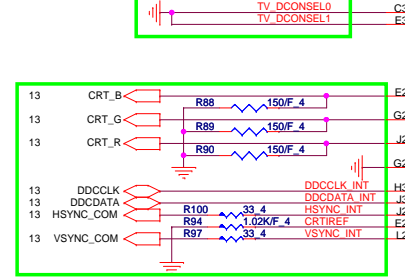
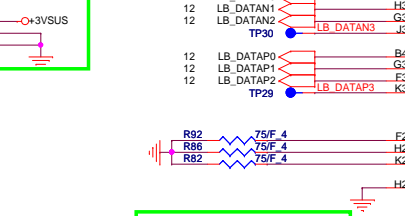
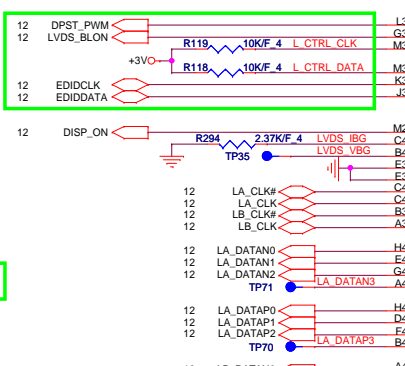
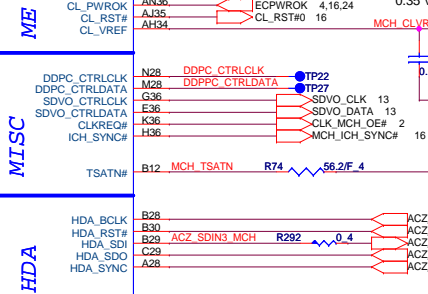
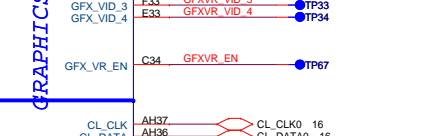
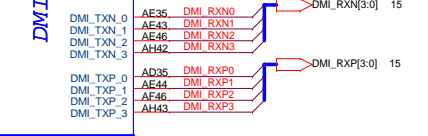
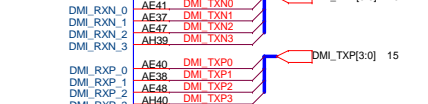
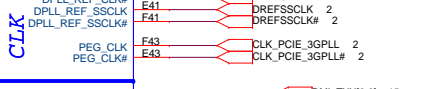
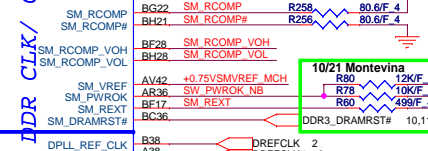
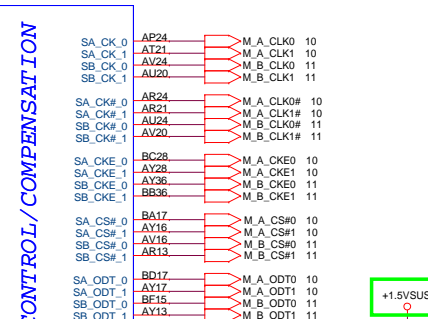
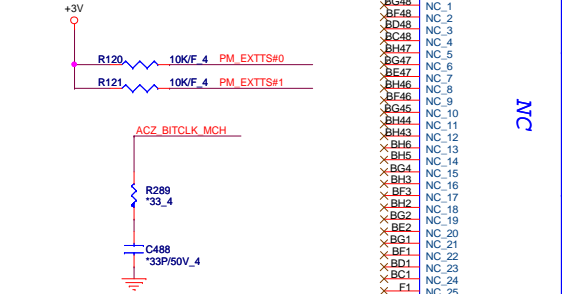
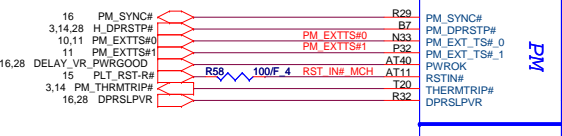
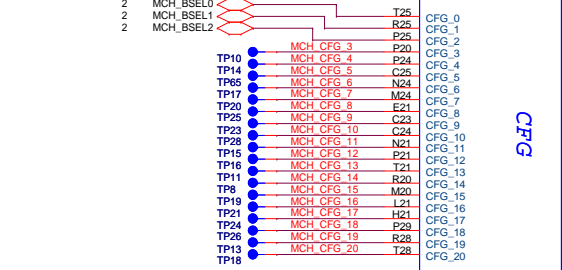
Low: ITPM Host Interface enabled
 High: ITPM Host Interface disabled (Default)
 MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)
 MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
 High: Disabled (Default)
 MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

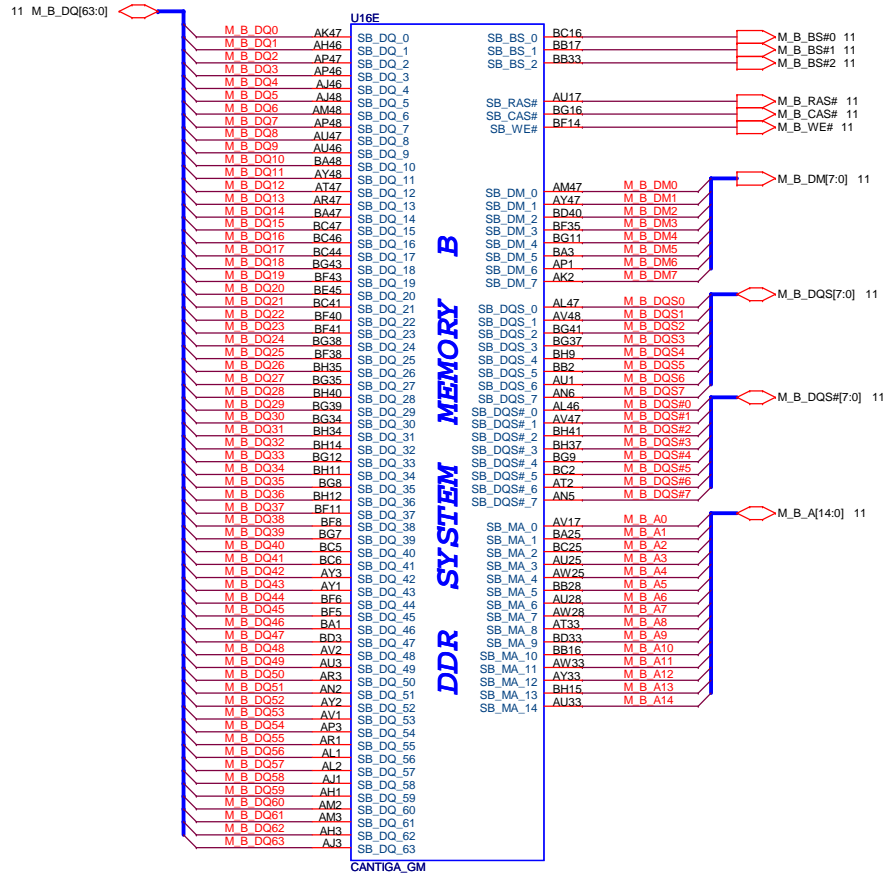
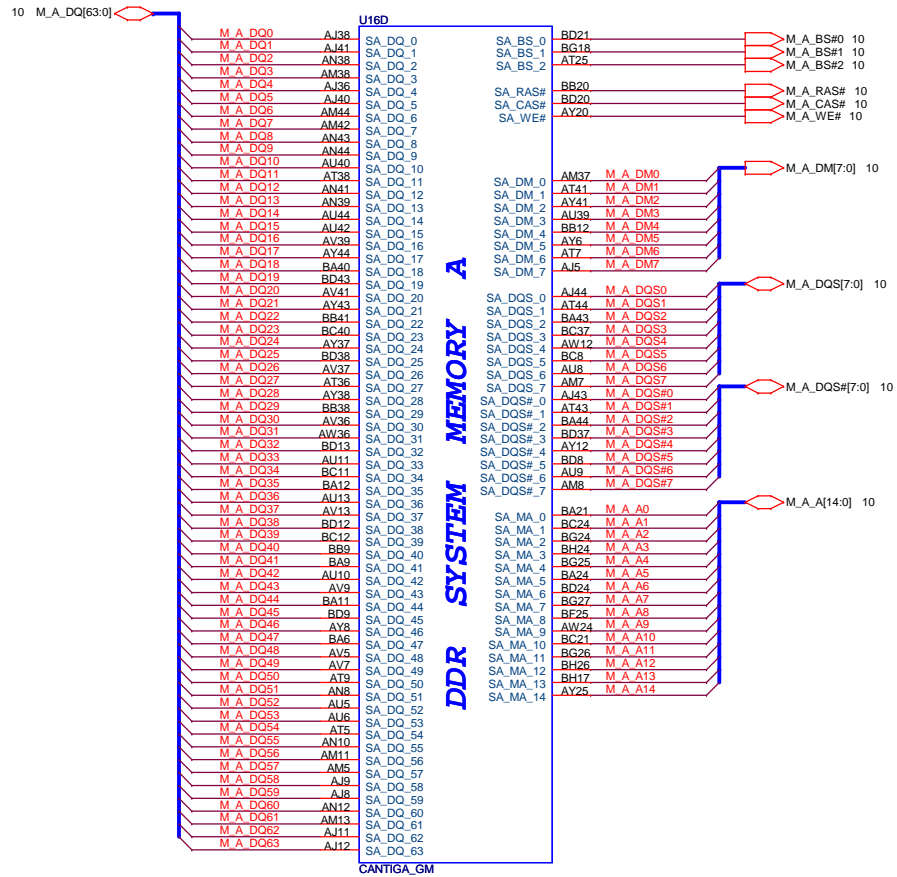
0	0	Reserved
0	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)



PROJECT : AX3
Quanta Computer Inc.

Size: Custom | Document Number: Cantiga DM/Display 2/5 | Rev: 1A
 Date: Friday, November 27, 2009 | Sheet: 6 of 30





10/21 Montevina +1.5VSUS

- AP33 VCC_SM_1
- BH32 VCC_SM_2
- BG32 VCC_SM_3
- BF32 VCC_SM_4
- BD32 VCC_SM_5
- BC32 VCC_SM_6
- BB32 VCC_SM_7
- BA32 VCC_SM_8
- AY32 VCC_SM_9
- AW32 VCC_SM_10
- AV32 VCC_SM_11
- AU32 VCC_SM_12
- AT32 VCC_SM_13
- AR32 VCC_SM_14
- AP32 VCC_SM_15
- AN32 VCC_SM_16
- AM32 VCC_SM_17
- AL32 VCC_SM_18
- AK32 VCC_SM_19
- AJ32 VCC_SM_20
- AI32 VCC_SM_21
- AH32 VCC_SM_22
- AG32 VCC_SM_23
- AF32 VCC_SM_24
- AE32 VCC_SM_25
- AD32 VCC_SM_26
- AC32 VCC_SM_27
- AB32 VCC_SM_28
- AA32 VCC_SM_29
- AY29 VCC_SM_30
- AW29 VCC_SM_31
- AU29 VCC_SM_32
- AT29 VCC_SM_33
- AR29 VCC_SM_34
- AP29 VCC_SM_35

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 designs.

- VCC_SM_36 BA36
- VCC_SM_37 BB24
- VCC_SM_38 BD16
- VCC_SM_40 AW16
- VCC_SM_42 AT13

U16G

- VCC_SM_1
- VCC_SM_2
- VCC_SM_3
- VCC_SM_4
- VCC_SM_5
- VCC_SM_6
- VCC_SM_7
- VCC_SM_8
- VCC_SM_9
- VCC_SM_10
- VCC_SM_11
- VCC_SM_12
- VCC_SM_13
- VCC_SM_14
- VCC_SM_15
- VCC_SM_16
- VCC_SM_17
- VCC_SM_18
- VCC_SM_19
- VCC_SM_20
- VCC_SM_21
- VCC_SM_22
- VCC_SM_23
- VCC_SM_24
- VCC_SM_25
- VCC_SM_26
- VCC_SM_27
- VCC_SM_28
- VCC_SM_29
- VCC_SM_30
- VCC_SM_31
- VCC_SM_32
- VCC_SM_33
- VCC_SM_34
- VCC_SM_35

VCC SM POWER

VCC GFX NCTF

- VCC_AXG_1
- VCC_AXG_2
- VCC_AXG_3
- VCC_AXG_4
- VCC_AXG_5
- VCC_AXG_6
- VCC_AXG_7
- VCC_AXG_8
- VCC_AXG_9
- VCC_AXG_10
- VCC_AXG_11
- VCC_AXG_12
- VCC_AXG_13
- VCC_AXG_14
- VCC_AXG_15
- VCC_AXG_16
- VCC_AXG_17
- VCC_AXG_18
- VCC_AXG_19
- VCC_AXG_20
- VCC_AXG_21
- VCC_AXG_22
- VCC_AXG_23
- VCC_AXG_24
- VCC_AXG_25
- VCC_AXG_26
- VCC_AXG_27
- VCC_AXG_28
- VCC_AXG_29
- VCC_AXG_30
- VCC_AXG_31
- VCC_AXG_32
- VCC_AXG_33
- VCC_AXG_34
- VCC_AXG_35
- VCC_AXG_36
- VCC_AXG_37
- VCC_AXG_38
- VCC_AXG_39
- VCC_AXG_40
- VCC_AXG_41
- VCC_AXG_42

VCC GFX

VCC SM LF

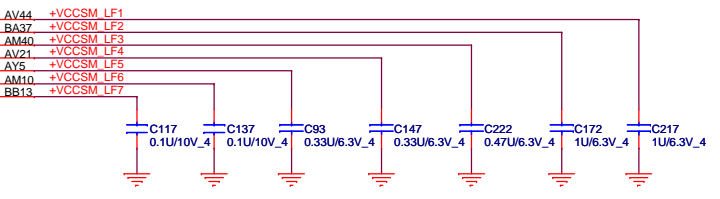
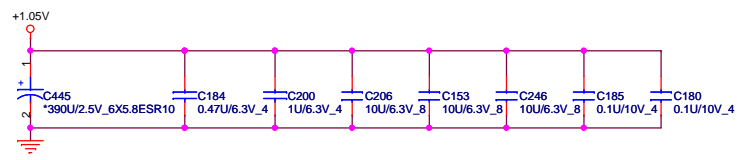
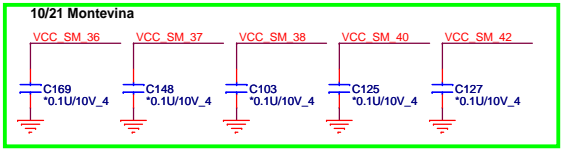
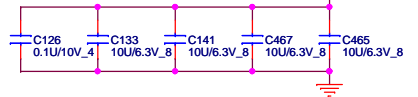
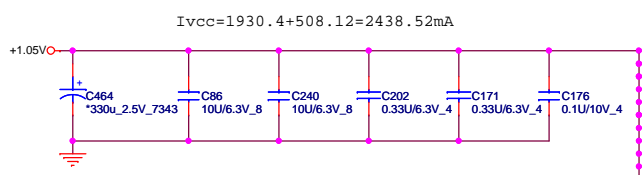
- VCC_AXG_SENSE AJ14
- VSS_AXG_SENSE AH14

CANTIGA_GM

- VCC_AXG_NCTF_1
- VCC_AXG_NCTF_2
- VCC_AXG_NCTF_3
- VCC_AXG_NCTF_4
- VCC_AXG_NCTF_5
- VCC_AXG_NCTF_6
- VCC_AXG_NCTF_7
- VCC_AXG_NCTF_8
- VCC_AXG_NCTF_9
- VCC_AXG_NCTF_10
- VCC_AXG_NCTF_11
- VCC_AXG_NCTF_12
- VCC_AXG_NCTF_13
- VCC_AXG_NCTF_14
- VCC_AXG_NCTF_15
- VCC_AXG_NCTF_16
- VCC_AXG_NCTF_17
- VCC_AXG_NCTF_18
- VCC_AXG_NCTF_19
- VCC_AXG_NCTF_20
- VCC_AXG_NCTF_21
- VCC_AXG_NCTF_22
- VCC_AXG_NCTF_23
- VCC_AXG_NCTF_24
- VCC_AXG_NCTF_25
- VCC_AXG_NCTF_26
- VCC_AXG_NCTF_27
- VCC_AXG_NCTF_28
- VCC_AXG_NCTF_29
- VCC_AXG_NCTF_30
- VCC_AXG_NCTF_31
- VCC_AXG_NCTF_32
- VCC_AXG_NCTF_33
- VCC_AXG_NCTF_34
- VCC_AXG_NCTF_35
- VCC_AXG_NCTF_36
- VCC_AXG_NCTF_37
- VCC_AXG_NCTF_38
- VCC_AXG_NCTF_39
- VCC_AXG_NCTF_40
- VCC_AXG_NCTF_41
- VCC_AXG_NCTF_42
- VCC_AXG_NCTF_43
- VCC_AXG_NCTF_44
- VCC_AXG_NCTF_45
- VCC_AXG_NCTF_46
- VCC_AXG_NCTF_47
- VCC_AXG_NCTF_48
- VCC_AXG_NCTF_49
- VCC_AXG_NCTF_50
- VCC_AXG_NCTF_51
- VCC_AXG_NCTF_52
- VCC_AXG_NCTF_53
- VCC_AXG_NCTF_54
- VCC_AXG_NCTF_55
- VCC_AXG_NCTF_56
- VCC_AXG_NCTF_57
- VCC_AXG_NCTF_58
- VCC_AXG_NCTF_59
- VCC_AXG_NCTF_60

- W28
- W26
- W26
- W25
- W25
- W24
- W24
- W23
- W23
- AM21
- AL21
- AK21
- W21
- V21
- U21
- AM20
- AK20
- W20
- U20
- AM19
- AL19
- AK19
- AJ19
- AG19
- AF19
- AE19
- AD19
- AA19
- Y19
- W19
- V19
- U19
- AM17
- AK17
- AH17
- AG17
- AK19
- AE17
- AJ26
- AC17
- AB17
- Y17
- W17
- V17
- AM16
- AL16
- AJ16
- AH16
- AG16
- AE16
- AC16
- AB16
- AA16
- Y16
- W16
- V16
- U16

Ivcc_axg=6326.84mA



U16F

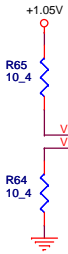
- VCC_1
- VCC_2
- VCC_3
- VCC_4
- VCC_5
- VCC_6
- VCC_7
- VCC_8
- VCC_9
- VCC_10
- VCC_11
- VCC_12
- VCC_13
- VCC_14
- VCC_15
- VCC_16
- VCC_17
- VCC_18
- VCC_19
- VCC_20
- VCC_21
- VCC_22
- VCC_23
- VCC_24
- VCC_25
- VCC_26
- VCC_27
- VCC_28
- VCC_29
- VCC_30
- VCC_31
- VCC_32
- VCC_33
- VCC_34
- VCC_35

VCC CORE POWER

VCC NCTF

- VCC_NCTF_1
- VCC_NCTF_2
- VCC_NCTF_3
- VCC_NCTF_4
- VCC_NCTF_5
- VCC_NCTF_6
- VCC_NCTF_7
- VCC_NCTF_8
- VCC_NCTF_9
- VCC_NCTF_10
- VCC_NCTF_11
- VCC_NCTF_12
- VCC_NCTF_13
- VCC_NCTF_14
- VCC_NCTF_15
- VCC_NCTF_16
- VCC_NCTF_17
- VCC_NCTF_18
- VCC_NCTF_19
- VCC_NCTF_20
- VCC_NCTF_21
- VCC_NCTF_22
- VCC_NCTF_23
- VCC_NCTF_24
- VCC_NCTF_25
- VCC_NCTF_26
- VCC_NCTF_27
- VCC_NCTF_28
- VCC_NCTF_29
- VCC_NCTF_30
- VCC_NCTF_31
- VCC_NCTF_32
- VCC_NCTF_33
- VCC_NCTF_34
- VCC_NCTF_35
- VCC_NCTF_36
- VCC_NCTF_37
- VCC_NCTF_38
- VCC_NCTF_39
- VCC_NCTF_40
- VCC_NCTF_41
- VCC_NCTF_42
- VCC_NCTF_43
- VCC_NCTF_44

CANTIGA_GM



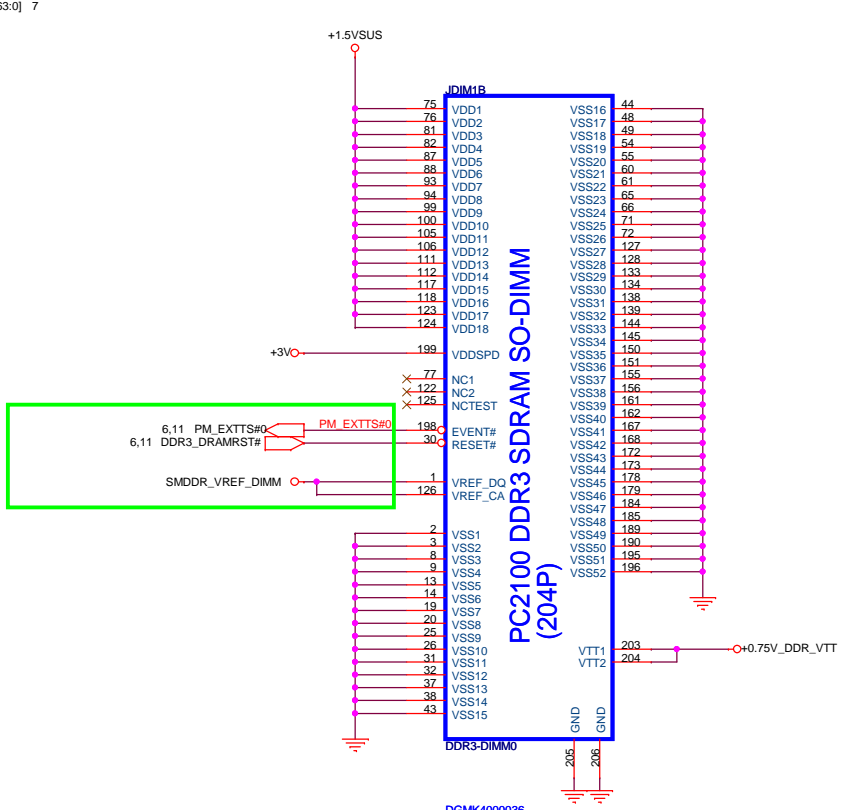
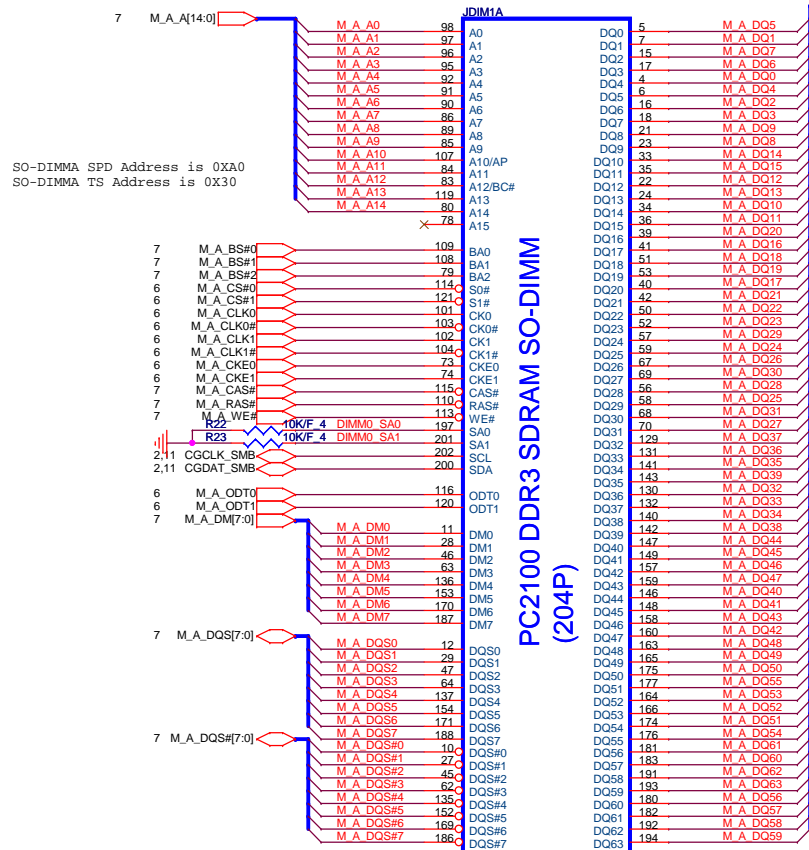
2,3,4,5,6,9,14,17,27,28 +1.05V
6,9,10,11,29,30 +1.5VSUS

PROJECT :AX3
Quanta Computer Inc.

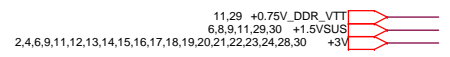
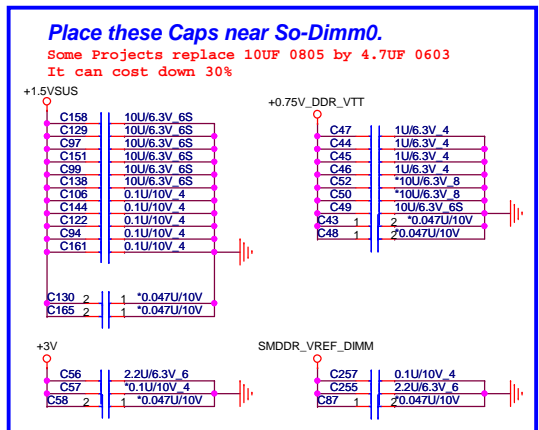
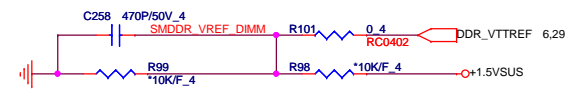
NB5

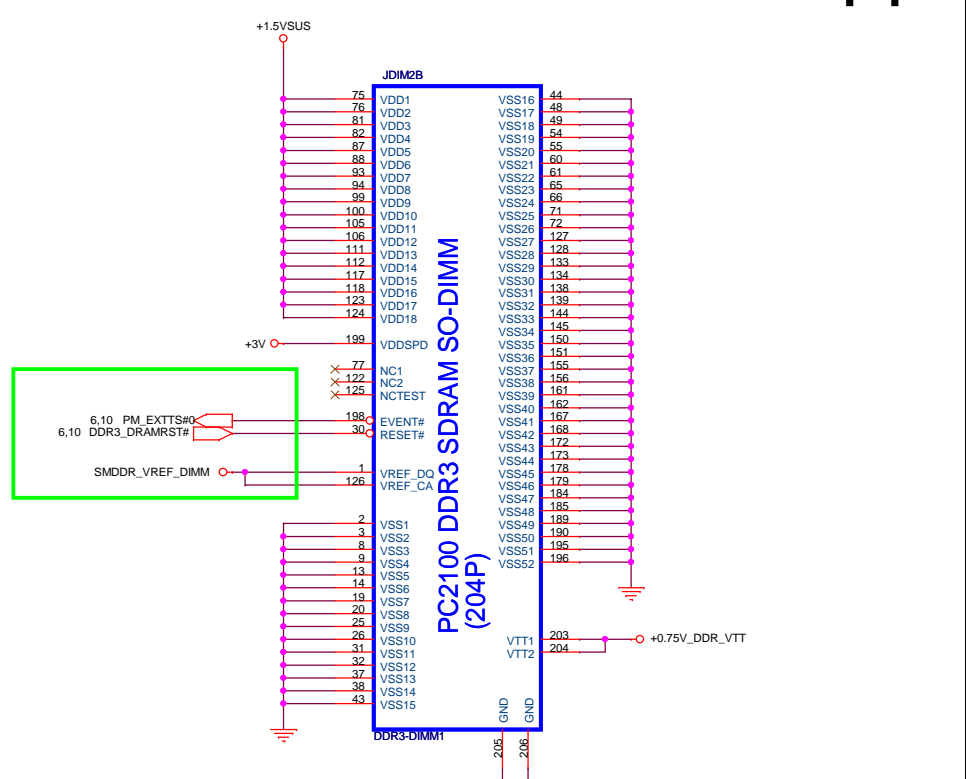
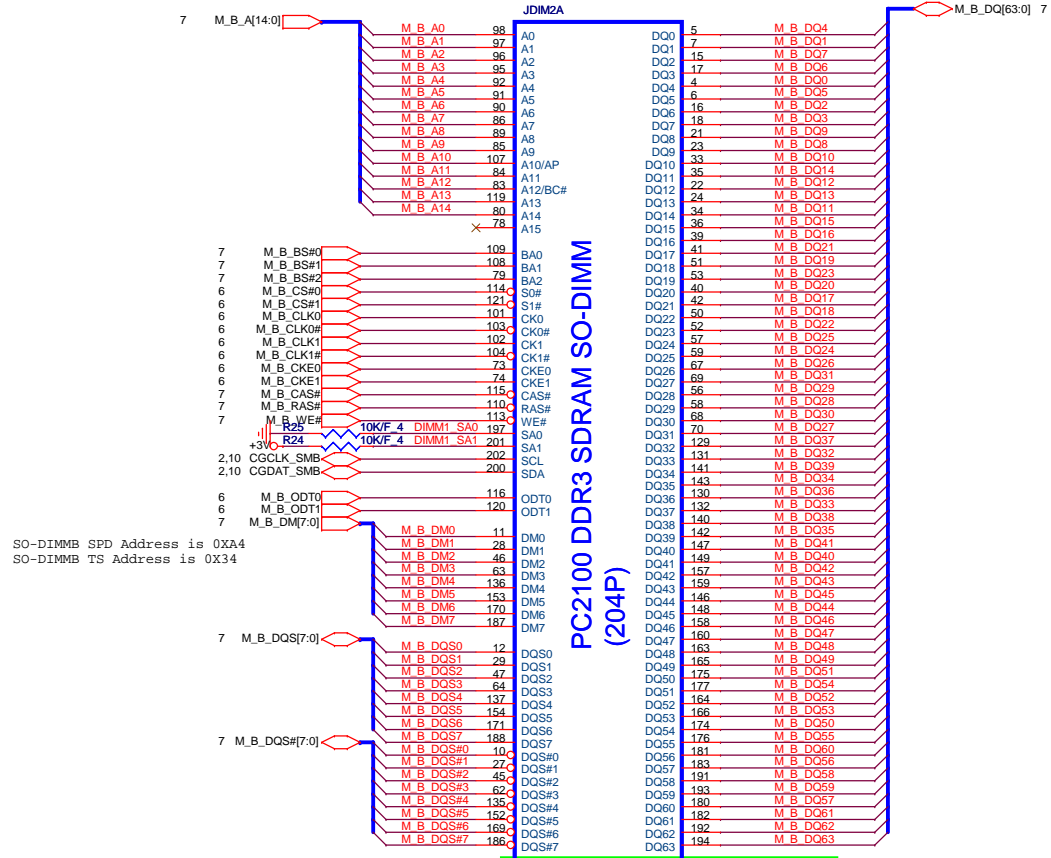
Size Custom Document Number Cantiga VCC 4/5 Rev 1A

Date: Friday, November 27, 2009 Sheet 8 of 30



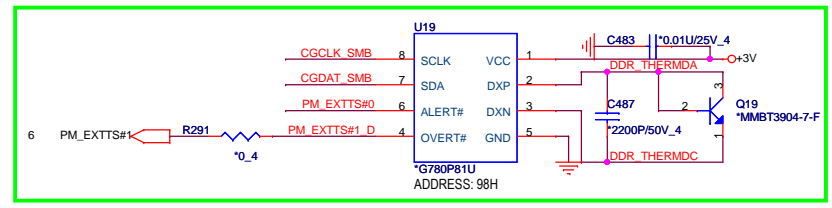
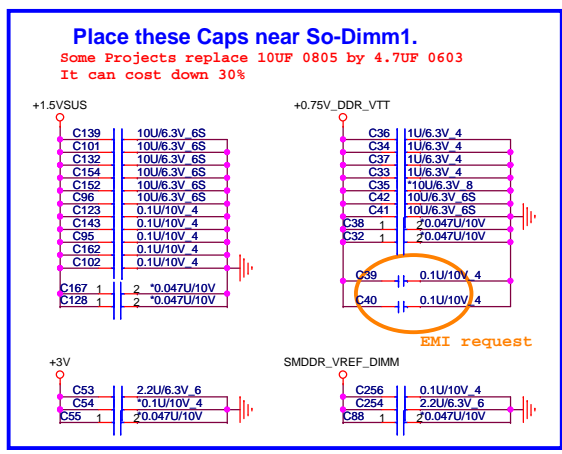
DDR3-DIMM0
DGMK4000036
IC SOCKET DDR3 SO-DIMM(204P,H9.2)
ddr-c-2013310-204p-1
Reverse type change to Standard type.





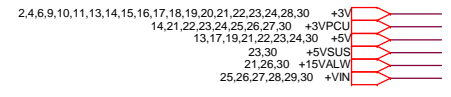
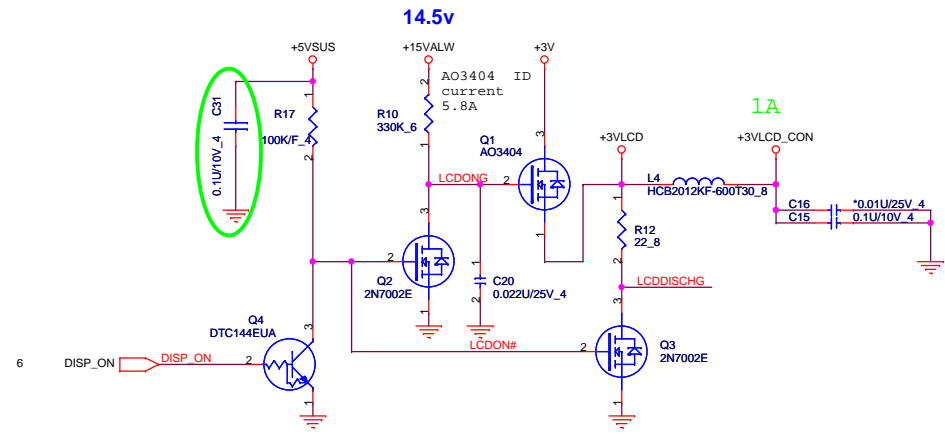
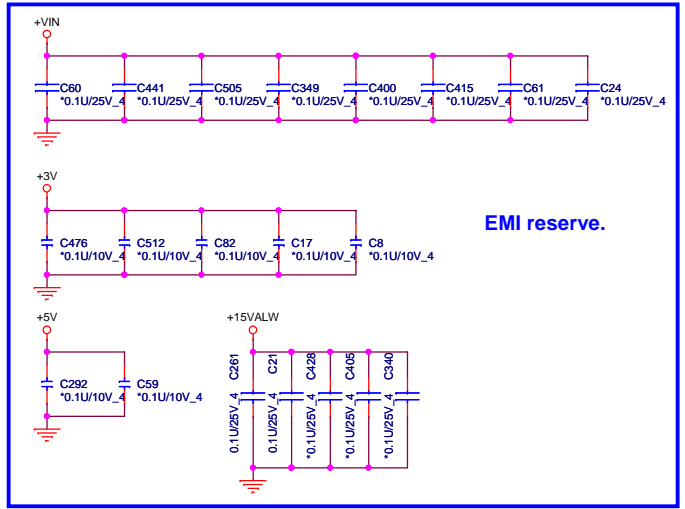
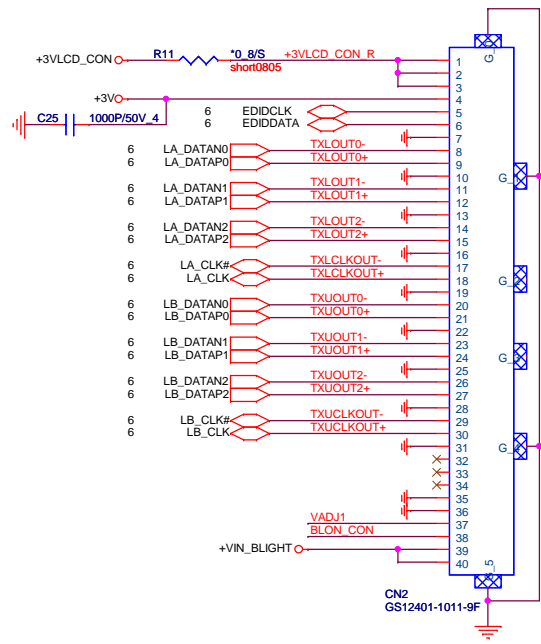
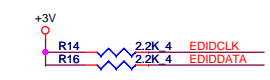
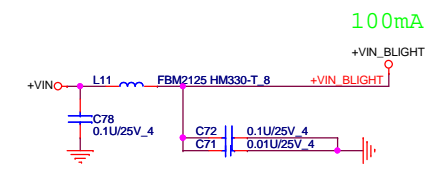
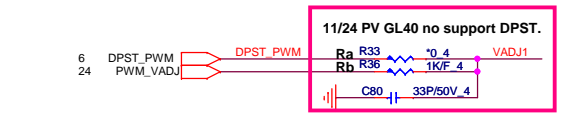
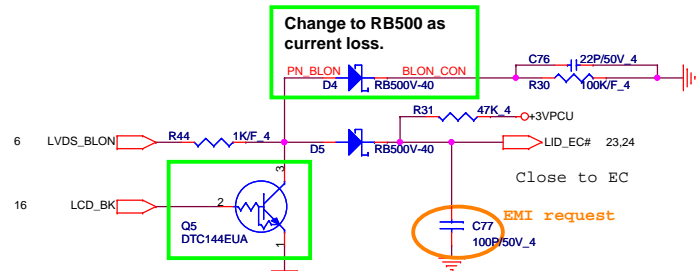
IC SOCKET DDR3 SO-DIMM(204P,H5.2)
ddr-c-2013289-204p

DDR3-DIMM1
DGMM4000037
IC SOCKET DDR3 SO-DIMM(204P,H5.2)
ddr-c-2013289-204p
Reverse type change to Standard type.

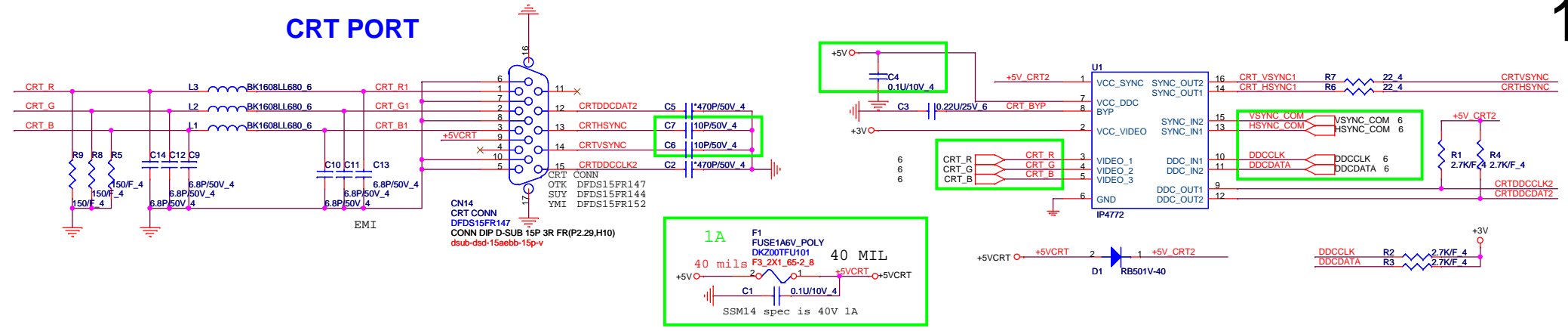


10,29 +0.75V_DDR_VTT
6,8,9,10,29,30 +1.5VSUS
2,4,6,9,10,12,13,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V

LID Switch



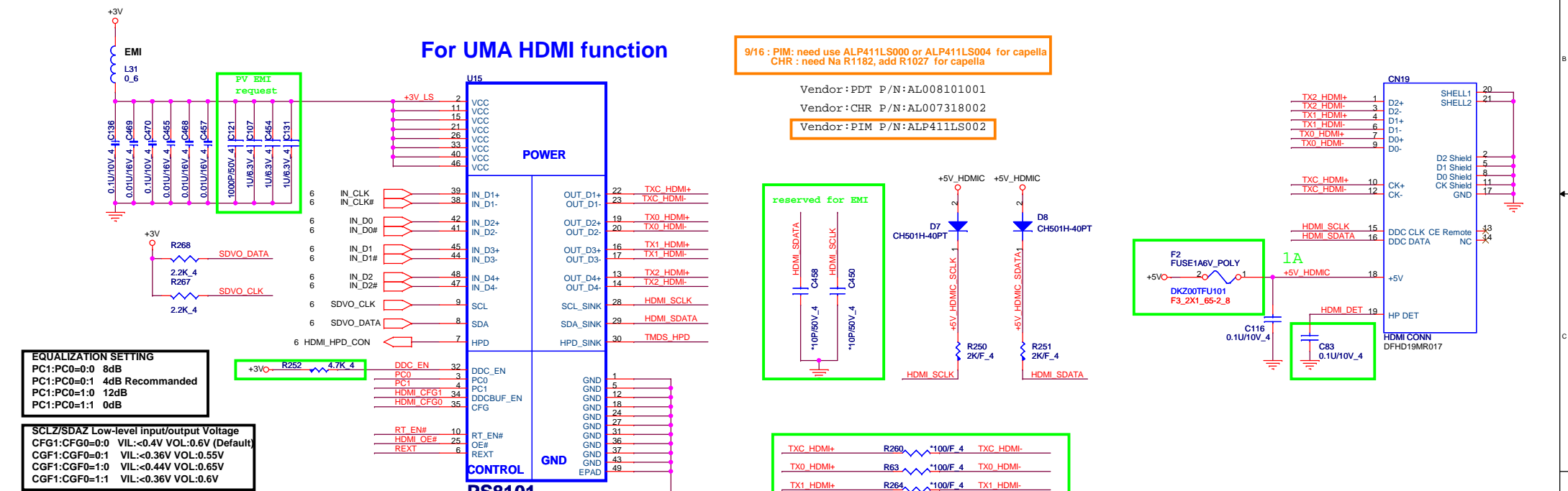
CRT PORT



For UMA HDMI function

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella
CHR : need Na R1182, add R1027 for capella

Vendor: PDT P/N: AL008101001
Vendor: CHR P/N: AL007318002
Vendor: PIM P/N: ALP411LS002



EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:-0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:-0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:-0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:-0.36V VOL:0.6V

Signals	R	PDT	CHR	PIM
PC0	Ra	4.7K	NC	NC
	Rb	NC	NC	0
PC1	Rc	NC	10K	NC
	Rd	NC	NC	0
HDMI_CFG0	Re	NC	10K	NC
	Rf	NC	NC	0
HDMI_CFG1	Rg	NC	10K	NC
	Rh	NC	NC	0
REXT	Ri	499	1.2K	0
RT_EN#	Rj	NC	NC	0
HDMI_OE#	Rk	NC	0	0

Detect	R	PDT	CHR	PIM
IC	Rm	0	20K	0
	Rn	NC	47K	NC
NB (Page6)	Ro	NC	20K	20K
	Rp	NC	7.5K	7.5K
	Rq	0	0	0

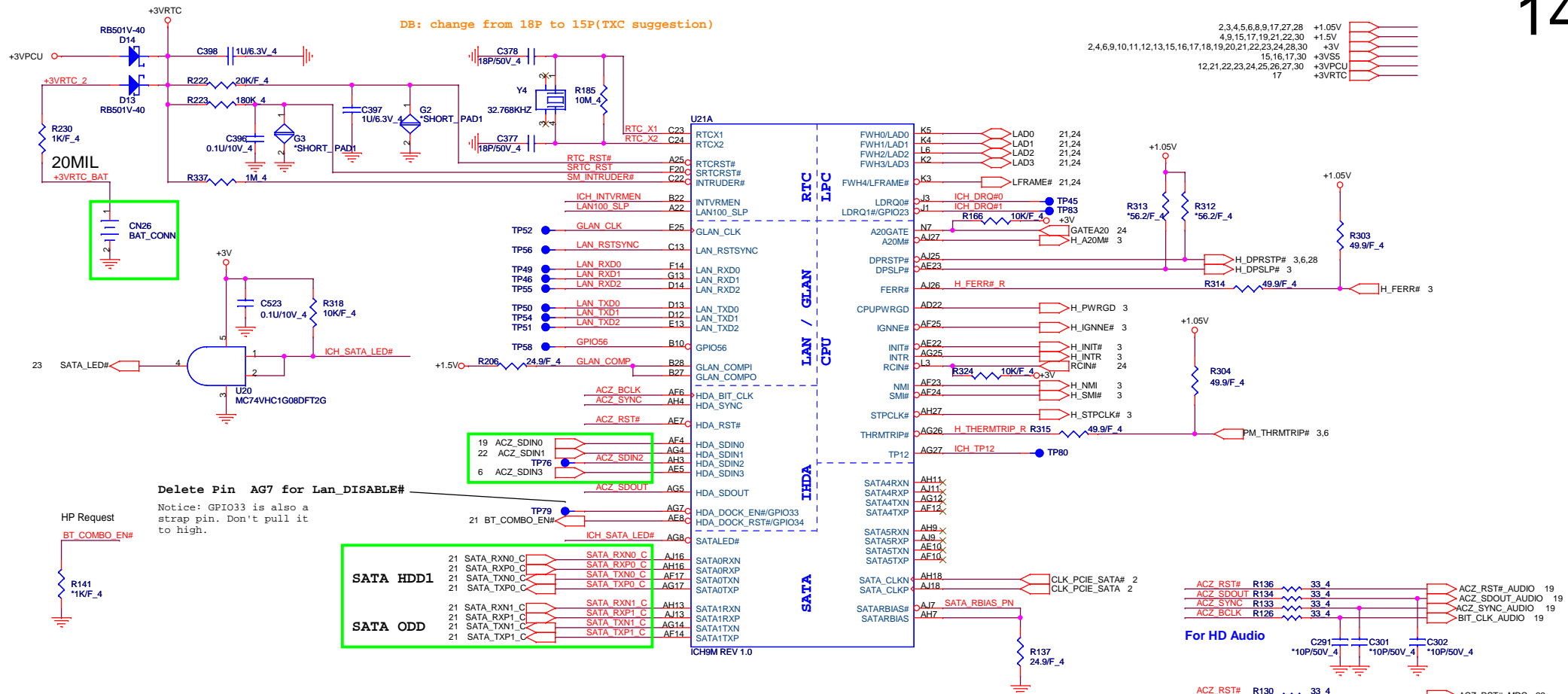
2,4,6,9,10,11,12,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V
12,17,19,21,22,23,24,30 +5V

PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number CRT/HDMI Conn Rev 1A

Date: Friday, November 27, 2009 Sheet 13 of 30

DB: change from 18P to 15P(TXC suggestion)

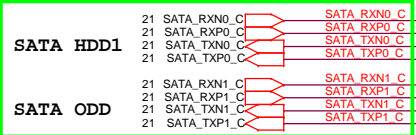


Delete Pin AG7 for Lan_DISABLE#

Notice: GPIO33 is also a strap pin. Don't pull it to high.

HP Request

BT_COMBO_EN#



SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN
Low = Internal VR disable
High = Internal VR enable(Default)

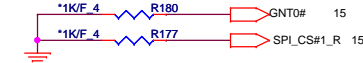
LAN100_SLP
Low = Internal VR disable
High = Internal VR enable(Default)

XOR Chain Entrance Strap

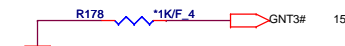
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

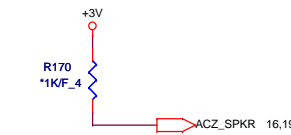
STRAP	PCI_GNT0#	SPI_CS#1	(default)
SPI	0	1	
PCI	1	0	
LPC	1	1	



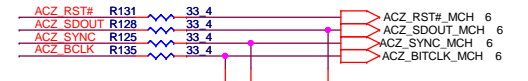
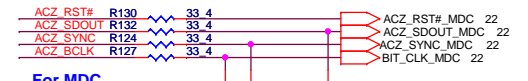
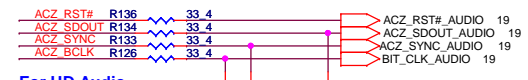
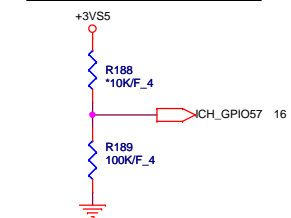
A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default



No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

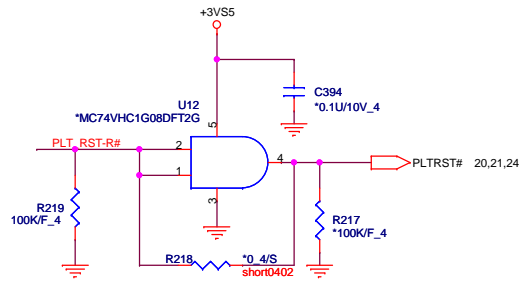
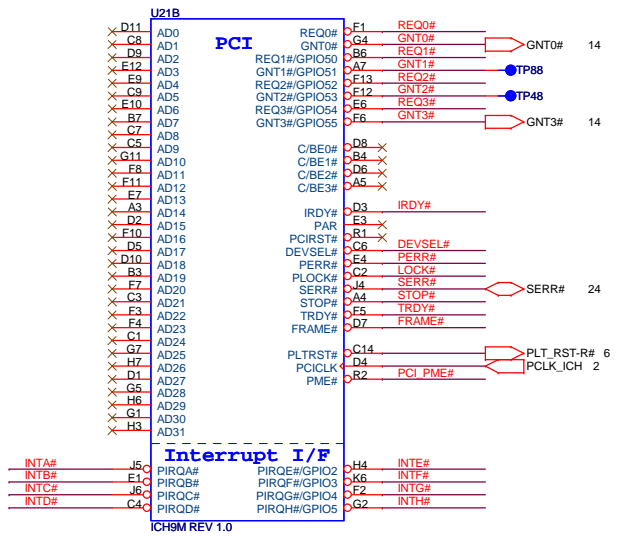
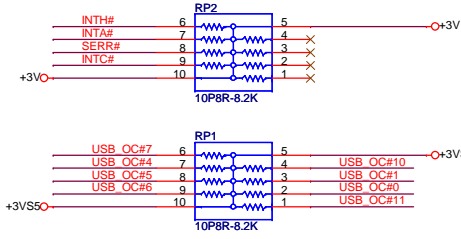
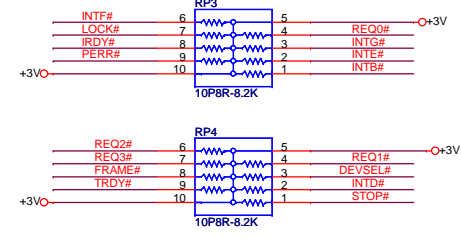
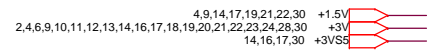
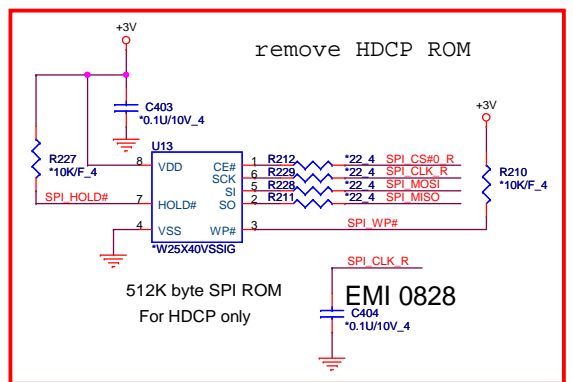
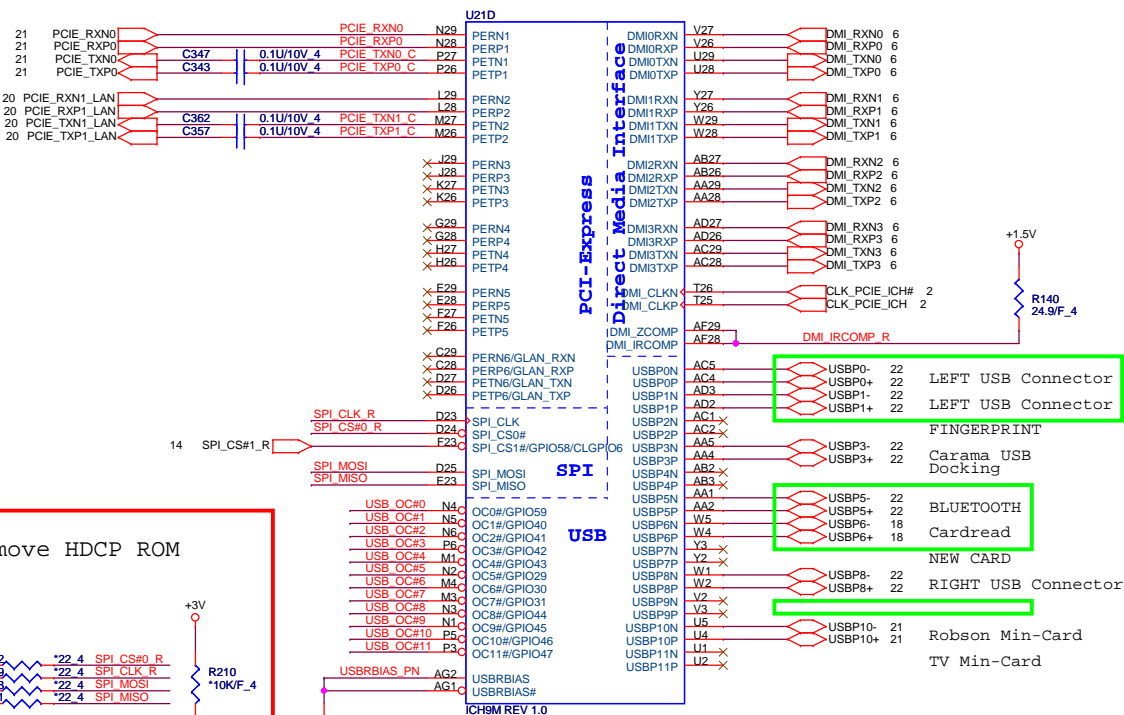


TPM physical presence	
ICH_GPIO57	Low: Default



MINI CARD PCI-E (WLAN)

PCI-E-LAN

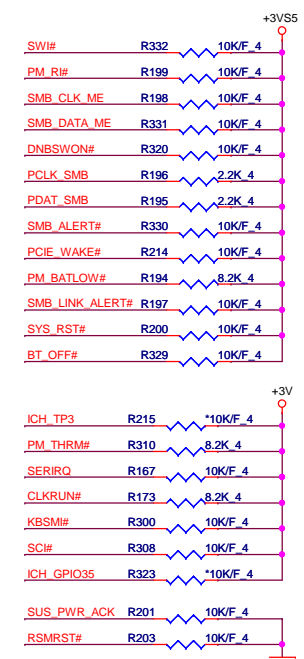
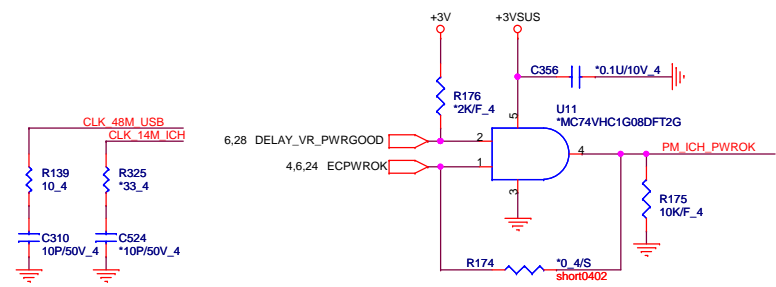
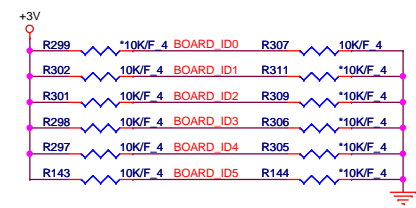
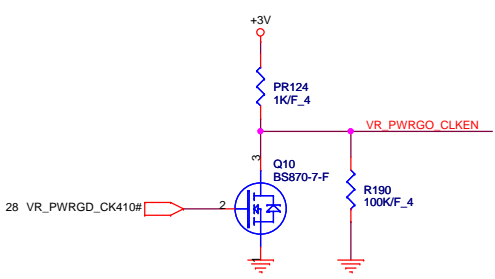
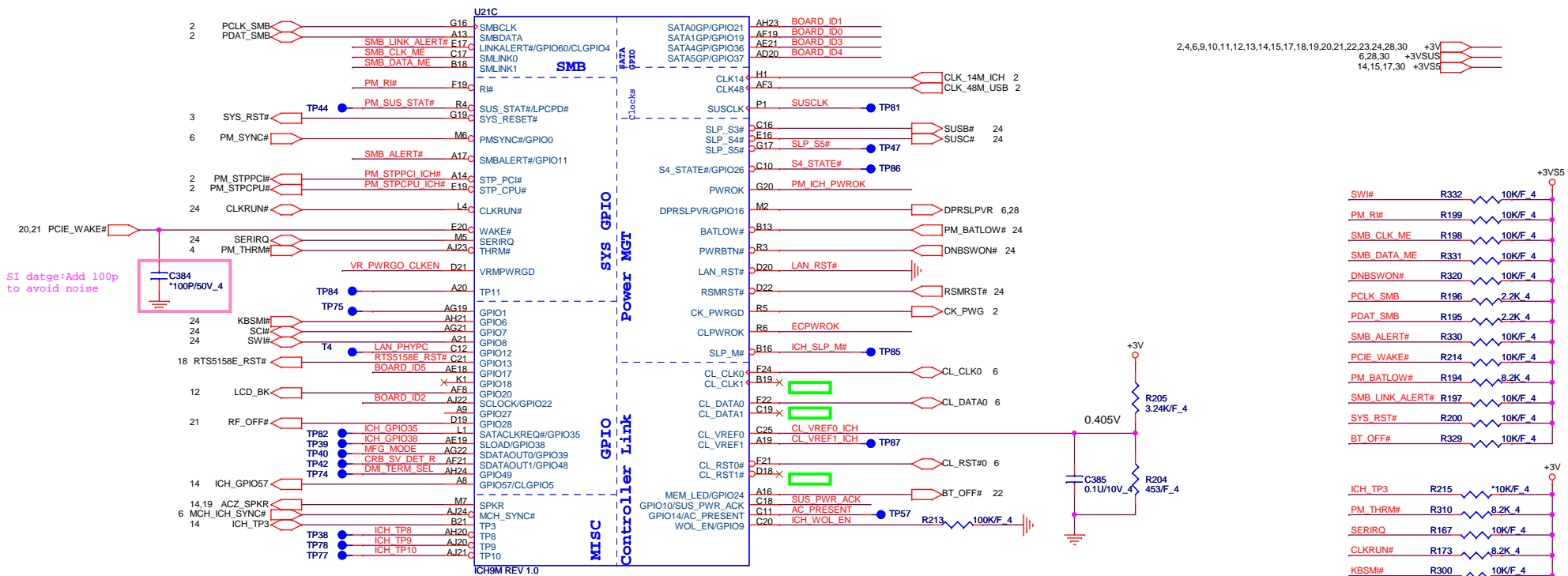


PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number ICH9-M DMI/PCIe/USB 2/4 Rev 1A

Date: Friday, November 27, 2009 Sheet 15 of 30

NB5



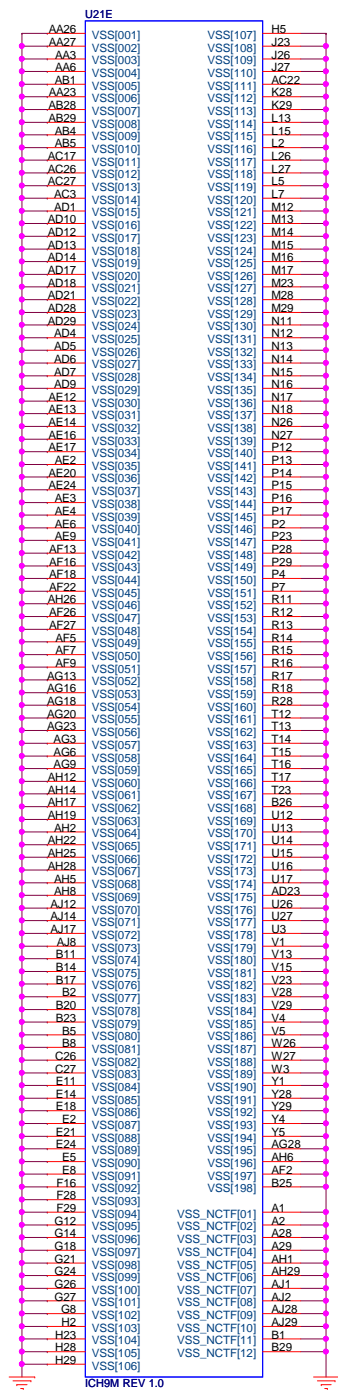
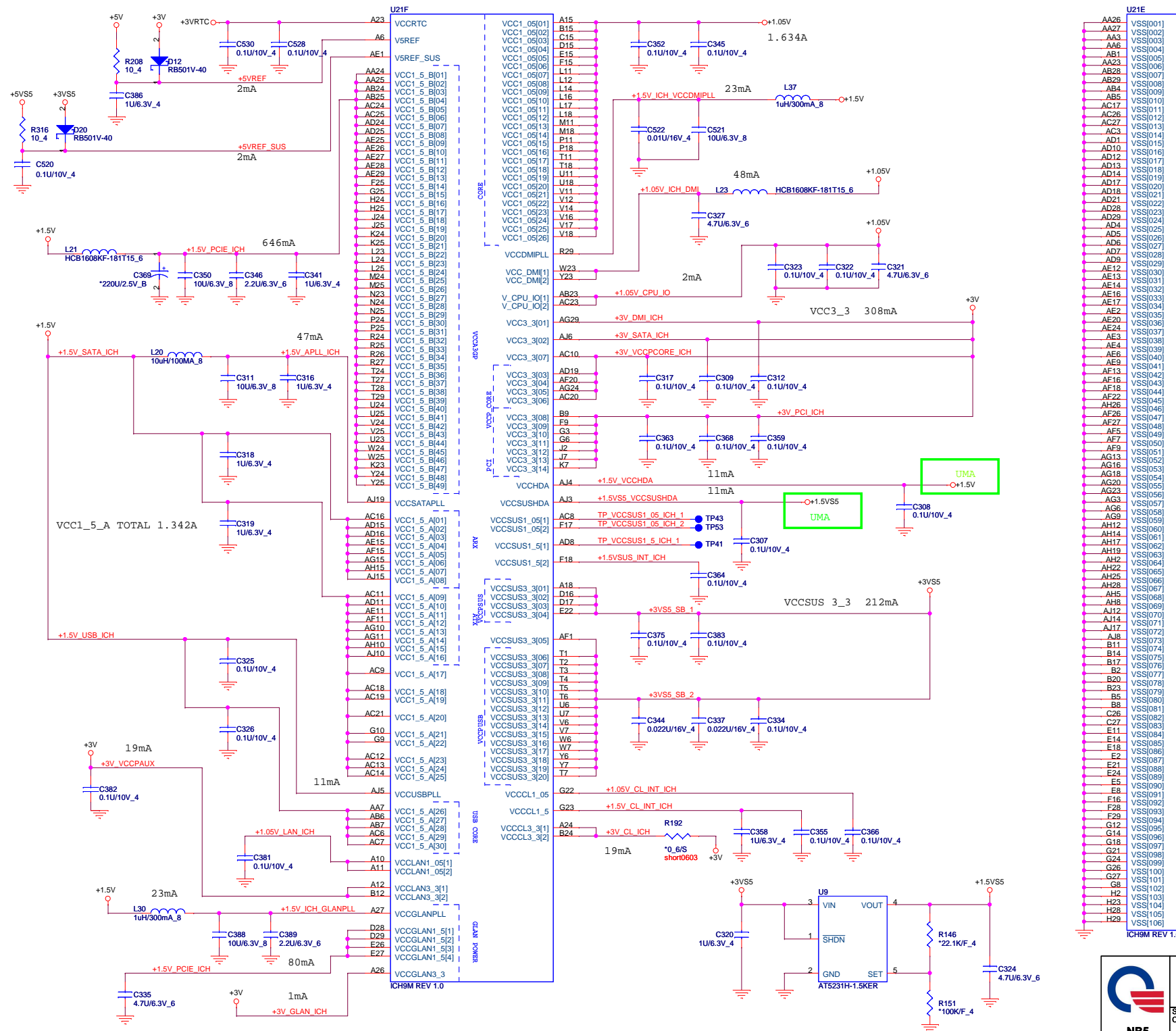
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
	GPIO19	GPIO21	GPIO22	GPIO36	GPIO37	GPIO17
UMA/DIS	0=UMA 1=Dis.					
CardReader		0=No 1=Yes				
HDMI			0=No 1=Yes			
Bluetooth				0=No 1=Yes		
Camera					0=No 1=Yes	
Modem						0=No 1=Yes

AX3 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
31AX6MB0000	0	1	1	1	1	1
31AX6MB0010	0	1	1	1	1	1
31AX6MB0020	0	1	1	1	1	1

PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number **ICH9-M GPIO/Board ID 3/4** Rev 1A

Date: Friday, November 27, 2009 Sheet 16 of 30

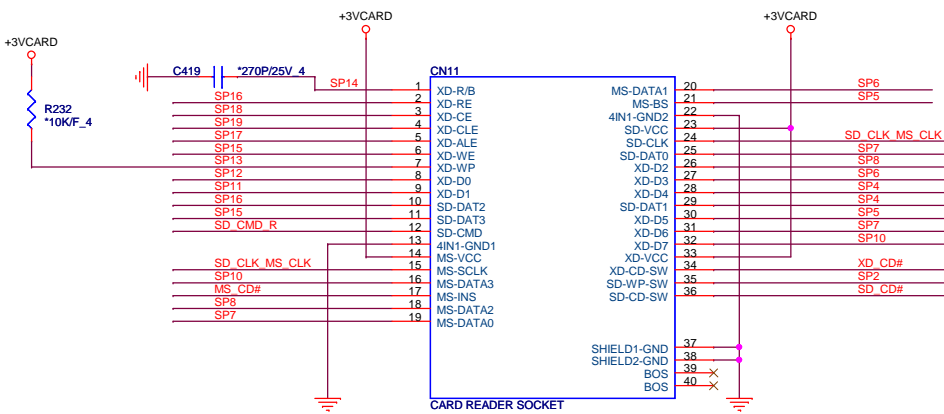
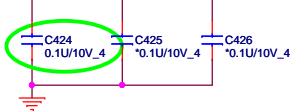
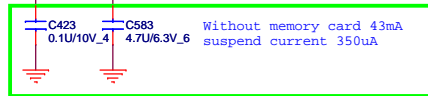
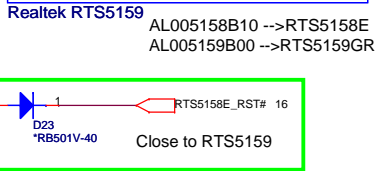
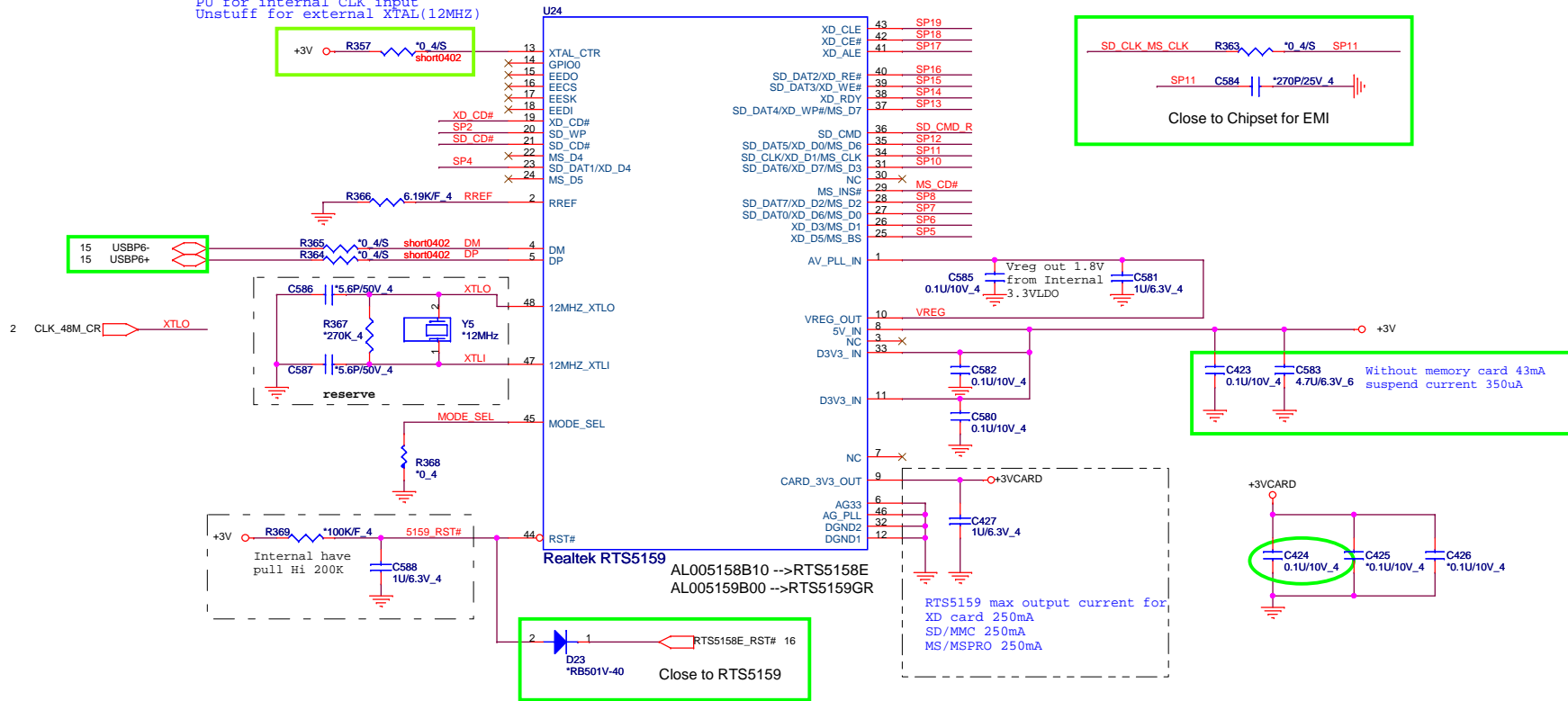


PROJECT :AX3
Quanta Computer Inc.

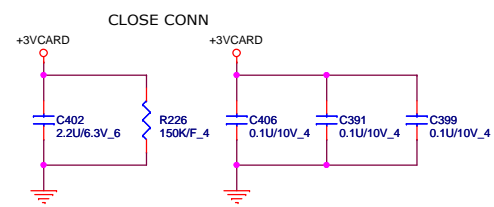
NB5 Size Custom Document Number ICH9-M Power 4/4 Rev 1A

Date: Thursday, November 26, 2009 | Sheet 17 of 30

PU for internal CLK input
Unstuff for external XTAL(12MHZ)



5 IN1 CARD-READER (PUSH-PUSH)
Support SD/SD PRO/MMC/MS/MS PRO/xD Cards



Note:

SP0	SD/MMC	MS	XD
SP1	SD_WP		XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

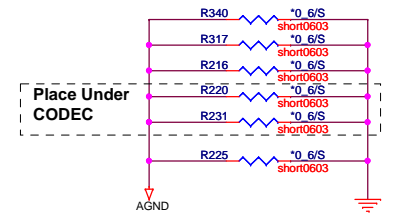
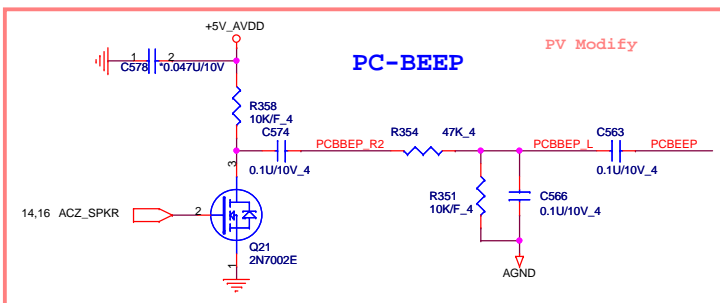
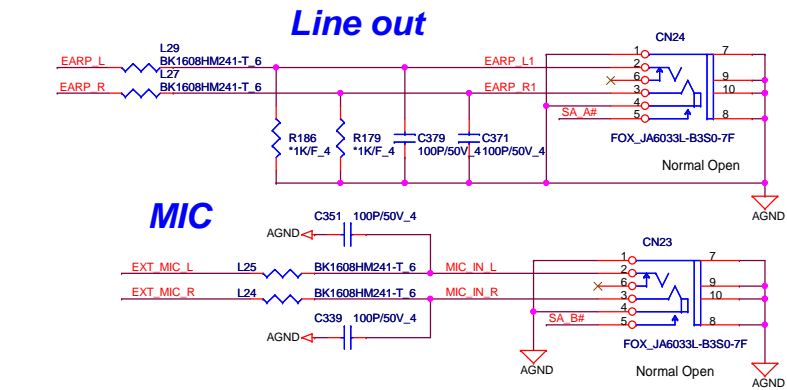
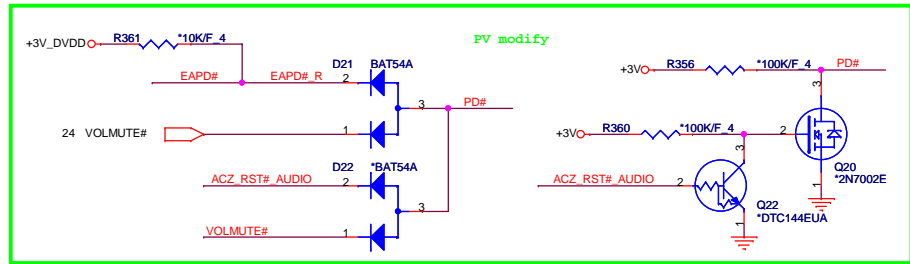
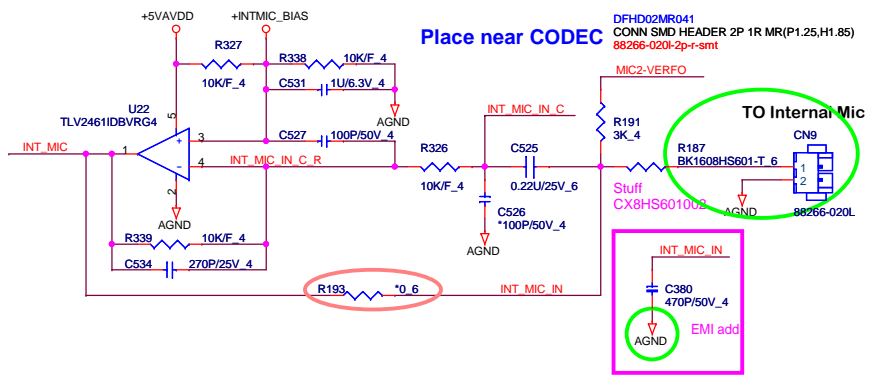
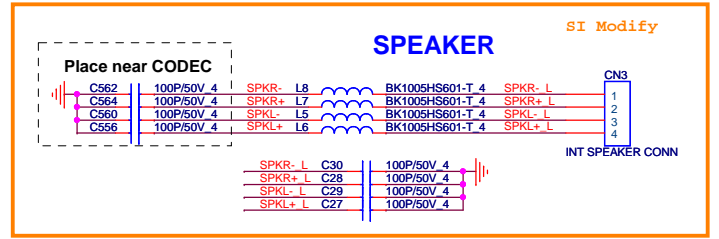
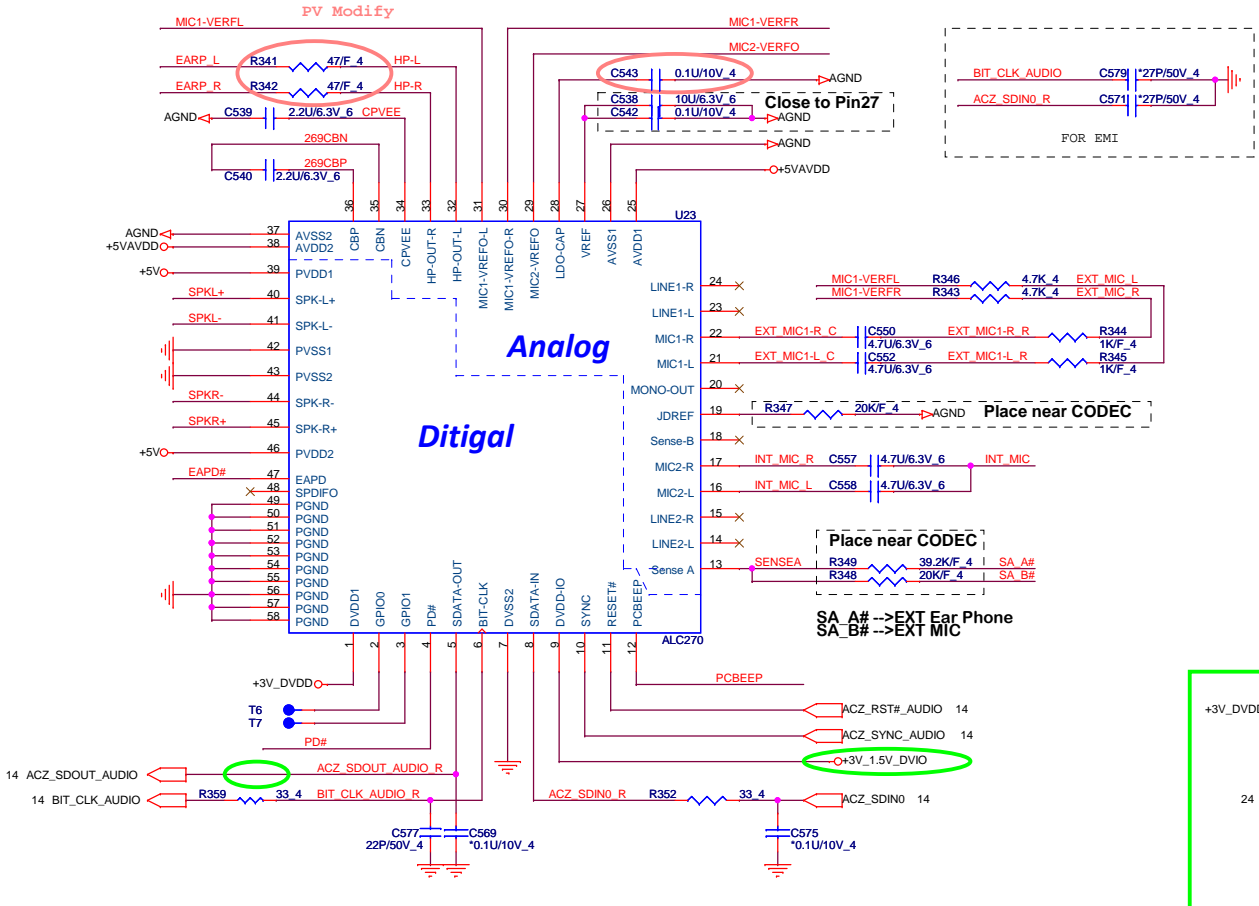
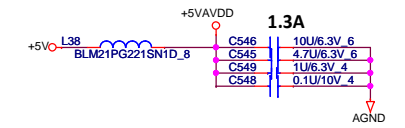
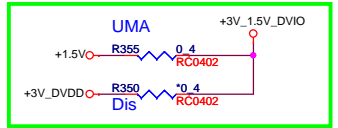
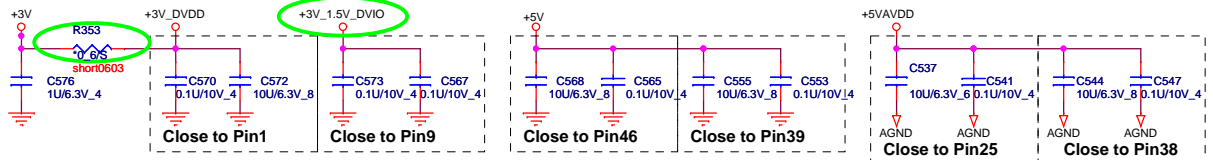
PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number
RTS5159/CR Socket

Date: Friday, November 27, 2009 Sheet 18 of 30

Rev 1A

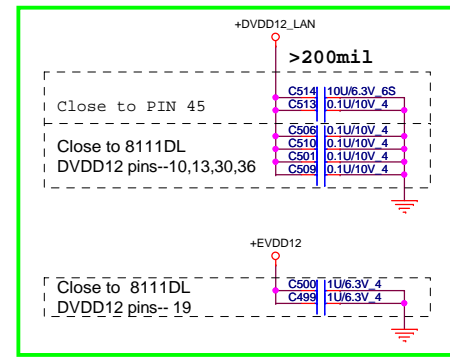
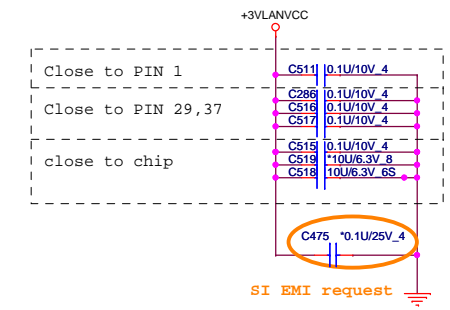
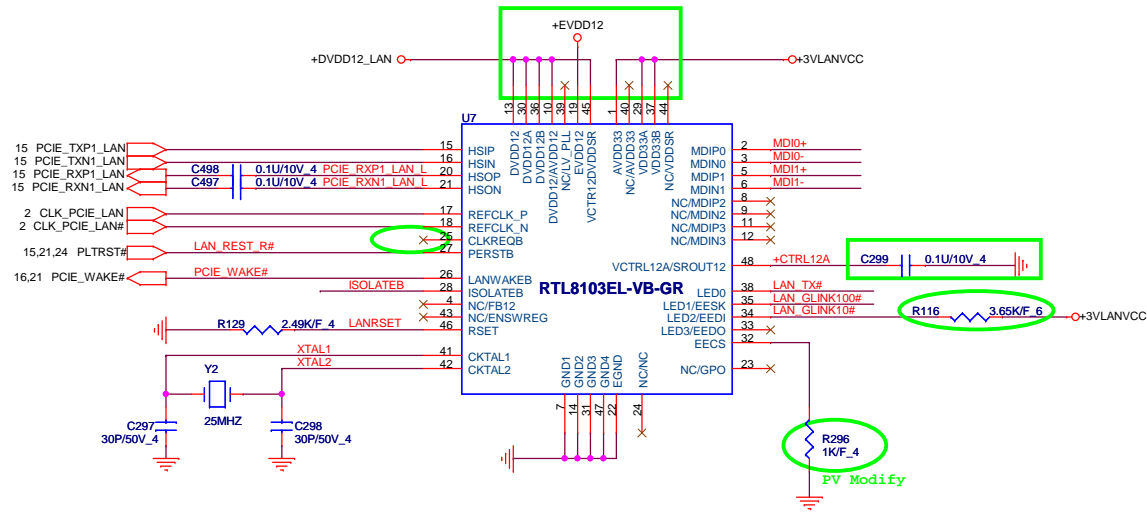
2,4,6,9,10,11,12,13,14,15,16,17,19,20,21,22,23,24,28,30 +3V



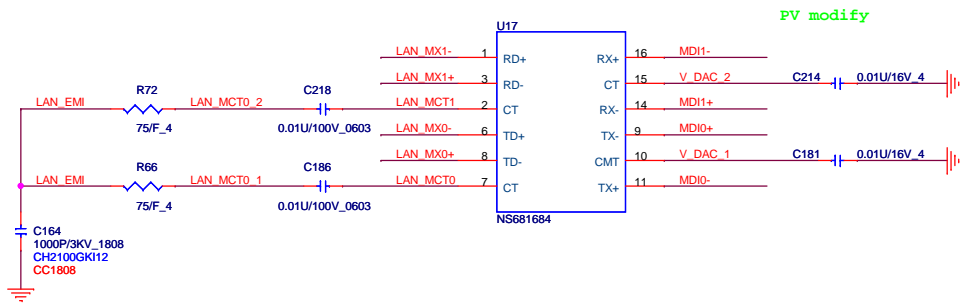
PROJECT :AX3
Quanta Computer Inc.

Size Custom Document Number **Azalia ALC270/Audio Jack** Rev 1A

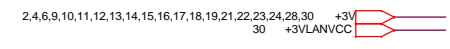
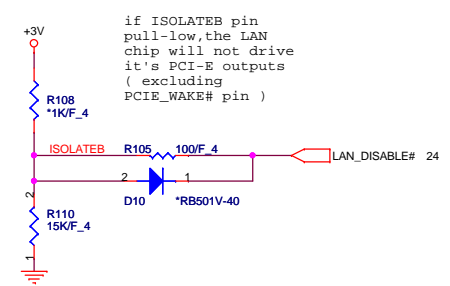
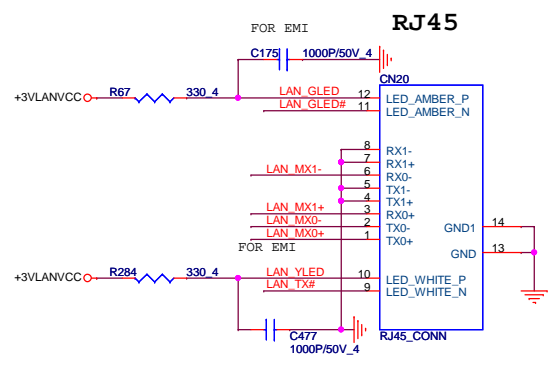
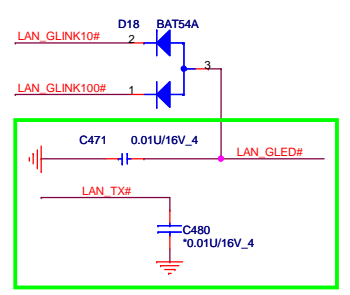
Date: Friday, November 27, 2009 Sheet 19 of 30



Transformer for 10/100



Lan Con.

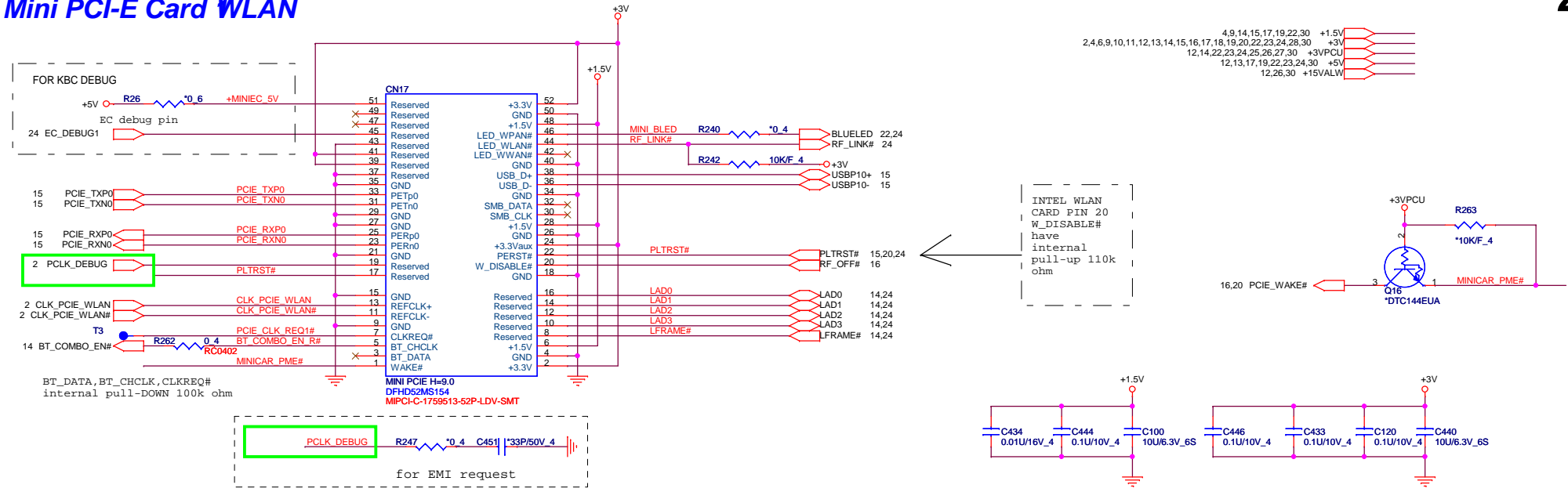


PROJECT :AX3
Quanta Computer Inc.

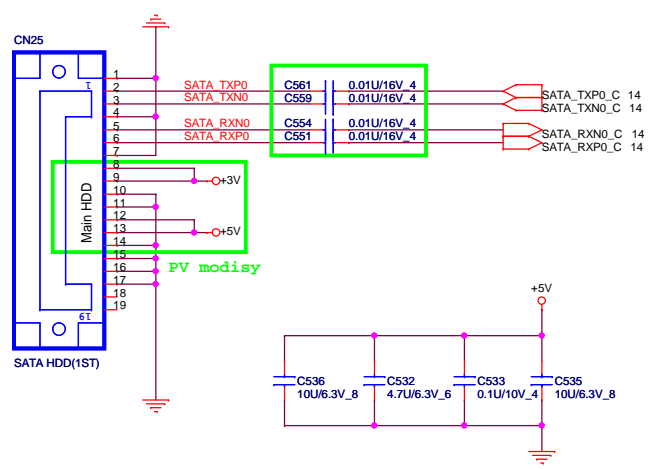
NBS Size Custom Document Number **RTL8103EL/RJ45** Rev 1A

Date: Friday, November 27, 2009 Sheet 20 of 30

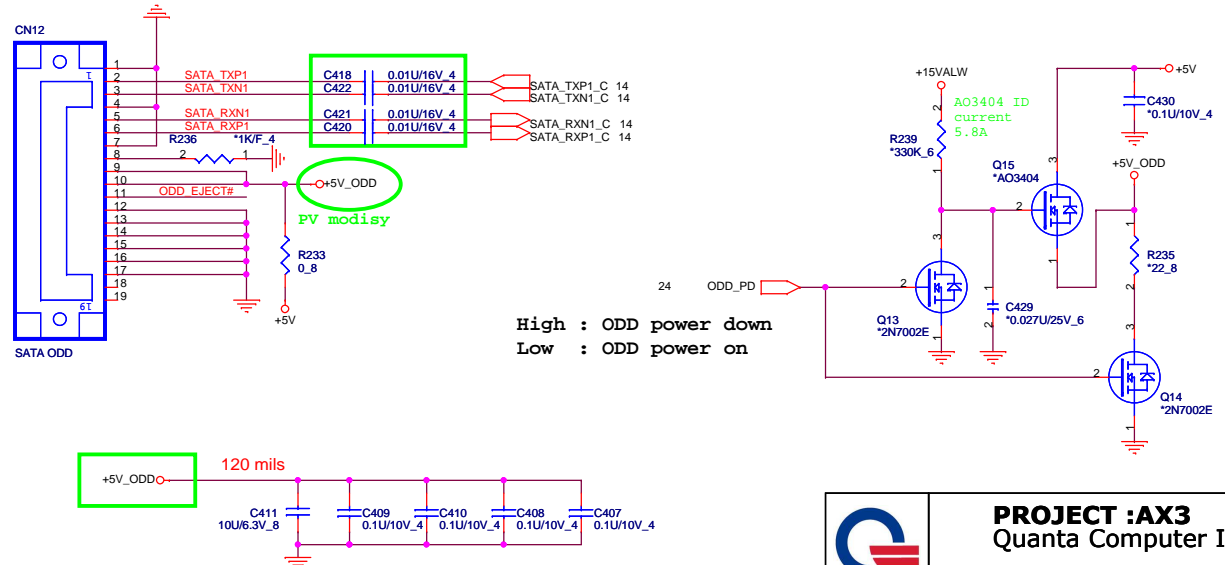
Mini PCI-E Card WLAN



SATA HDD CONNECTOR



SATA ODD CONNECTOR

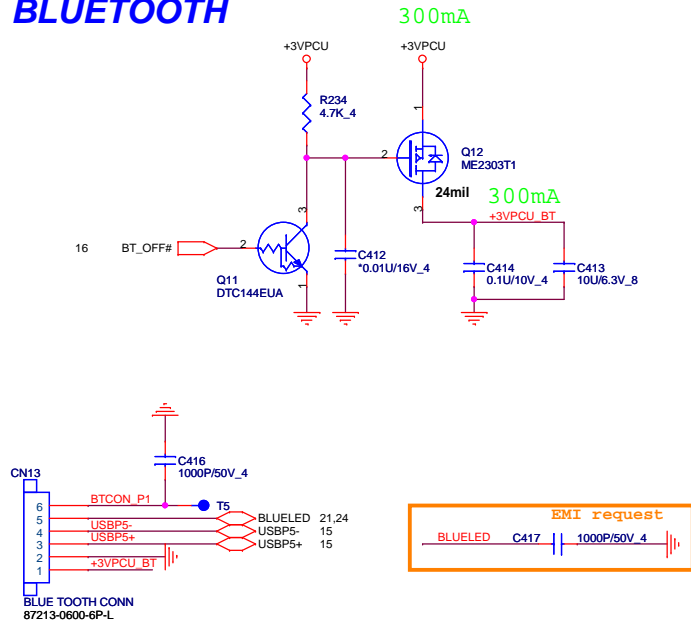


PROJECT :AX3
Quanta Computer Inc.

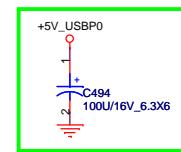
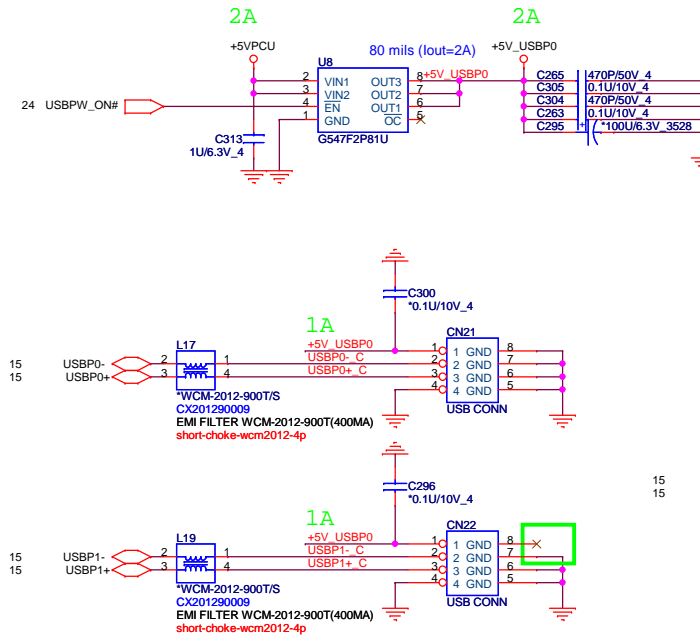
NBS5

Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Friday, November 27, 2009	Sheet 21 of 30	

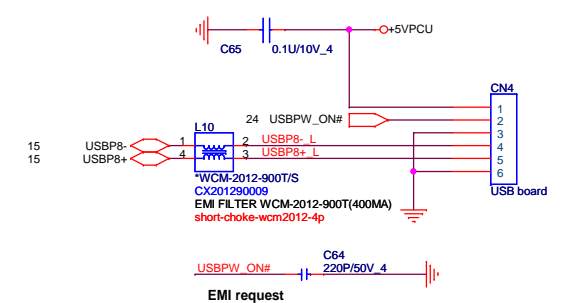
BLUETOOTH



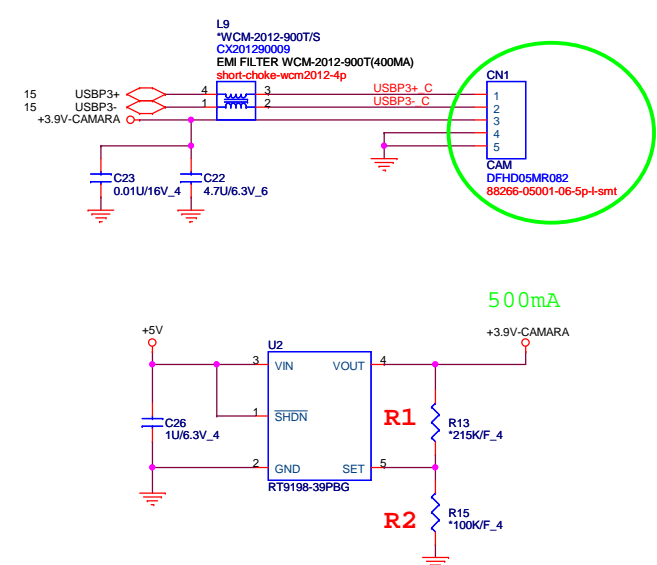
LEFT SIDE USBX1



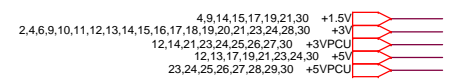
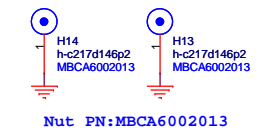
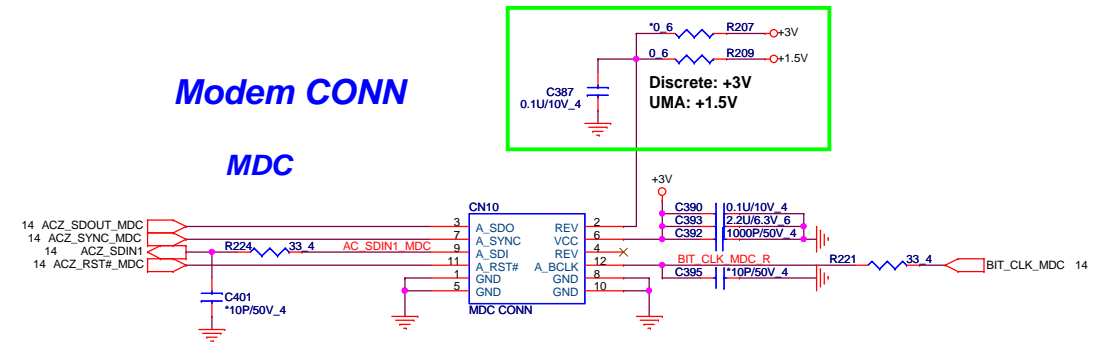
Right SIDE USBX1



CAMERA



Modem CONN

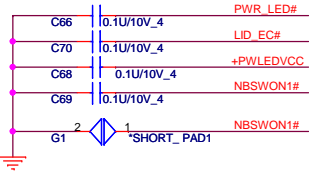
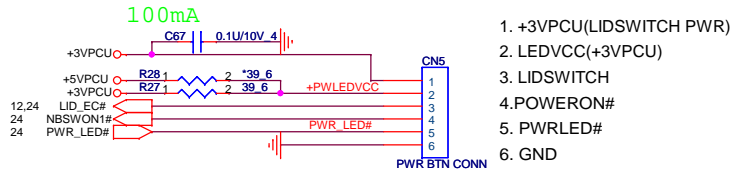


PROJECT :AX3
Quanta Computer Inc.

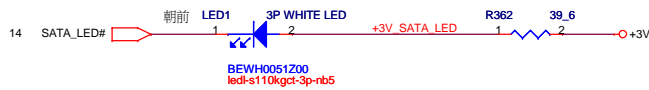
Size Custom Document Number **USB/BT/CAMERA/Modem** Rev 1A

NBS Date: Friday, November 27, 2009 Sheet 22 of 30

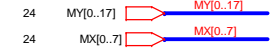
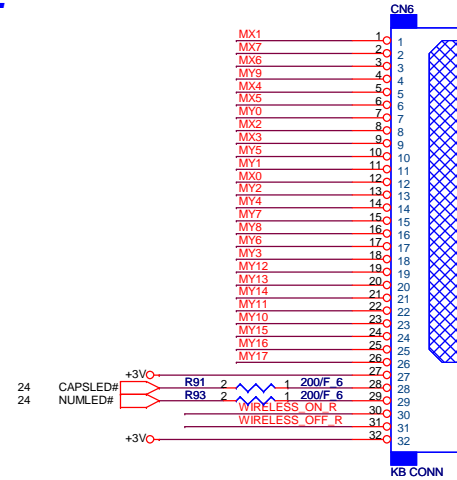
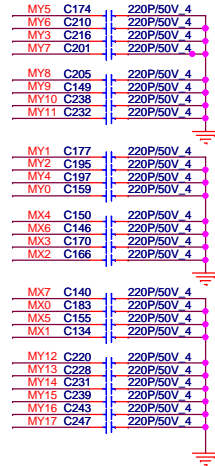
POWER BOTTON CONNECT



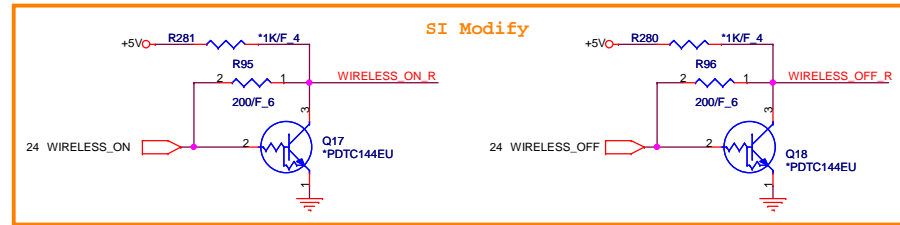
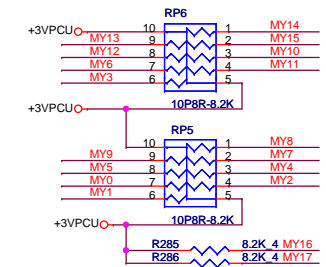
SATA LED



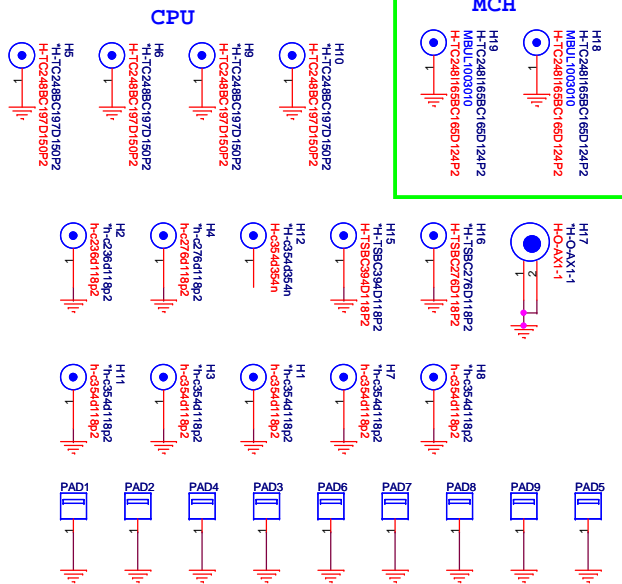
KEYBOARD Con.



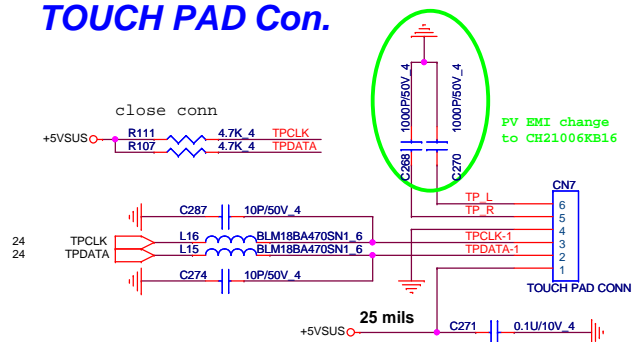
KEYBOARD PULL-UP



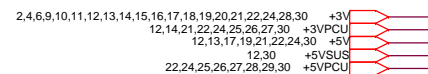
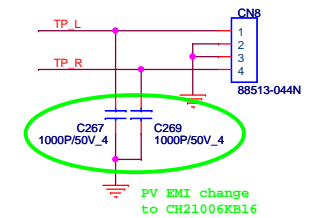
HOLE & PAD



TOUCH PAD Con.



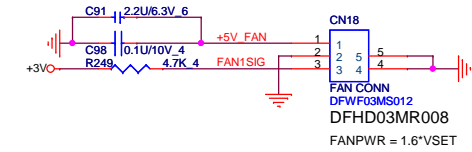
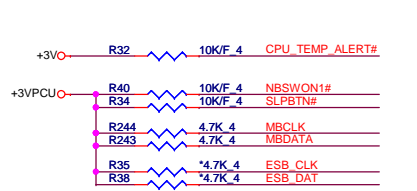
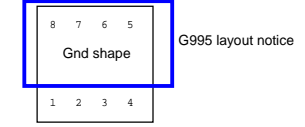
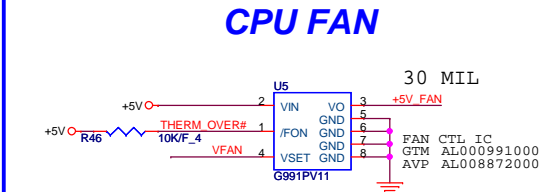
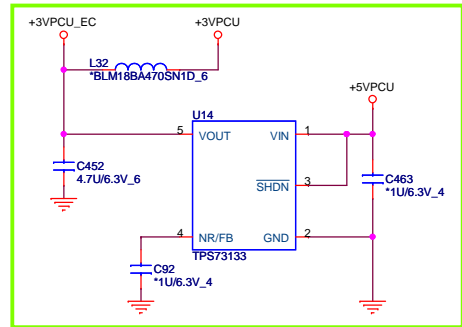
To TOUCH PAD SW board



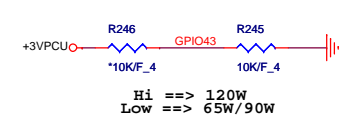
PROJECT :AX3

Quanta Computer Inc.

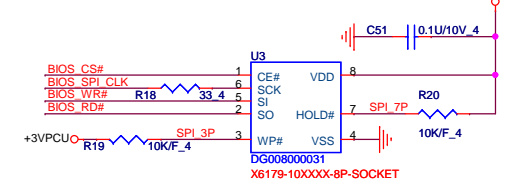
Size Custom	Document Number KB/TP/SW/LED/Hole	Rev 1A
Date: Friday, November 27, 2009		Sheet 23 of 30



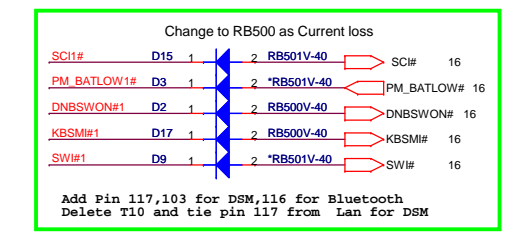
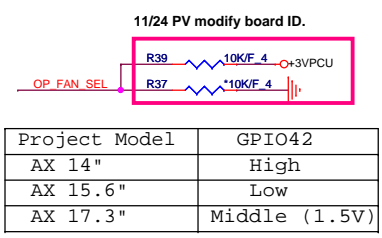
Adapter select for EC



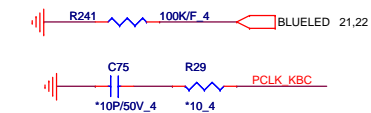
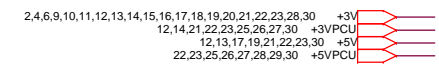
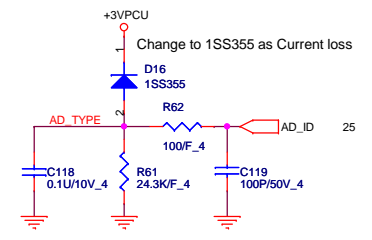
1M byte SPI EC ROM



GPIO42 control fan table



adapter Type check

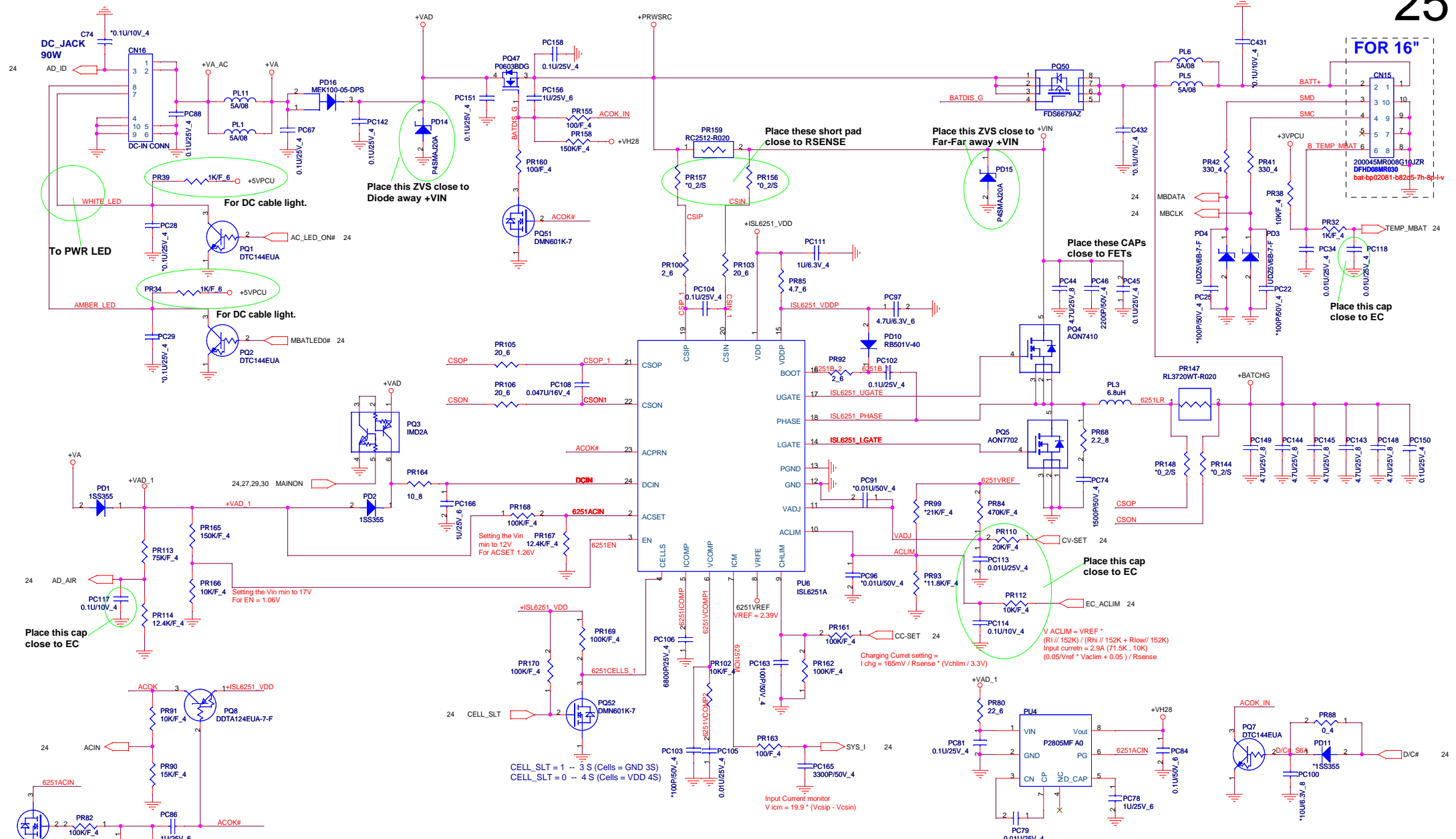



PROJECT :AX3

Quanta Computer Inc.

Rev 1A

Size Custom	Document Number EC (KB3926)/ROM	Rev 1A
Date: Friday, November 27, 2009		Sheet 24 of 30



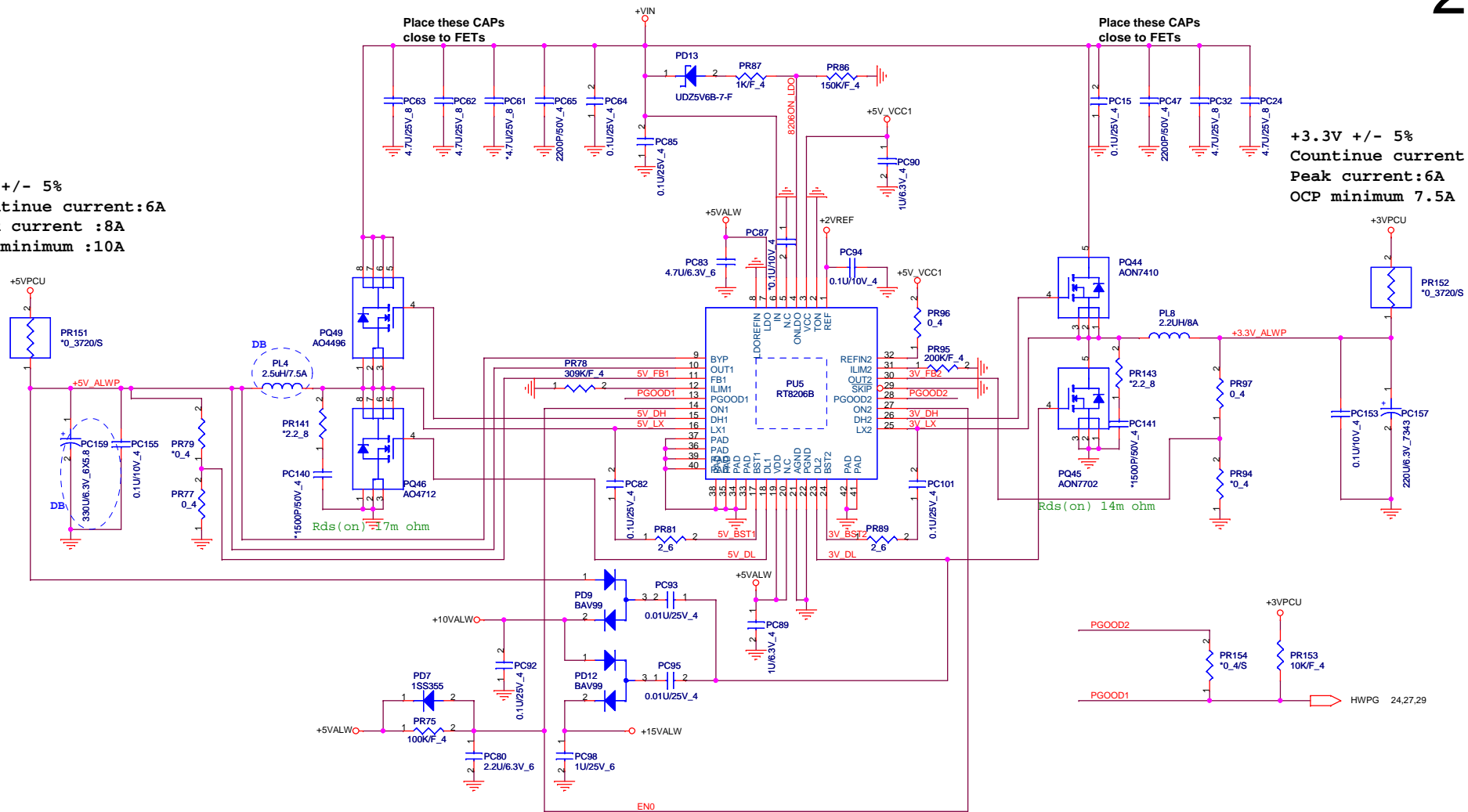
	PROJECT :AX3		Rev PV
	Quanta Computer Inc.		
	Size Custom	Document Number CHARGER (ISL6251)	
Date: Friday, November 27, 2009		Sheet 25 of 30	

+5V +/- 5%
 Countinue current:6A
 Peak current :8A
 OCP minimum :10A

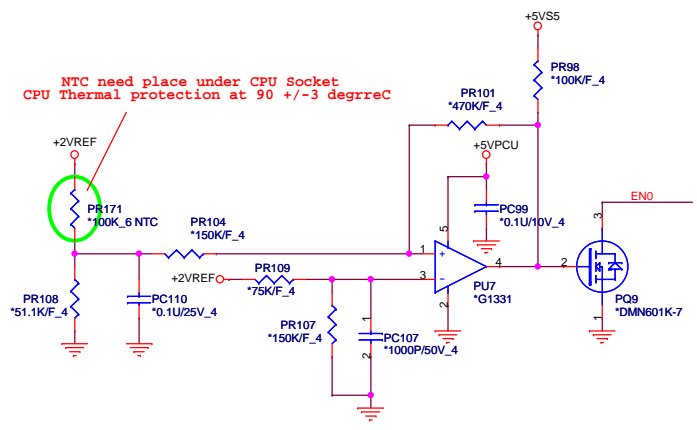
+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A

Place these CAPs
 close to FETs

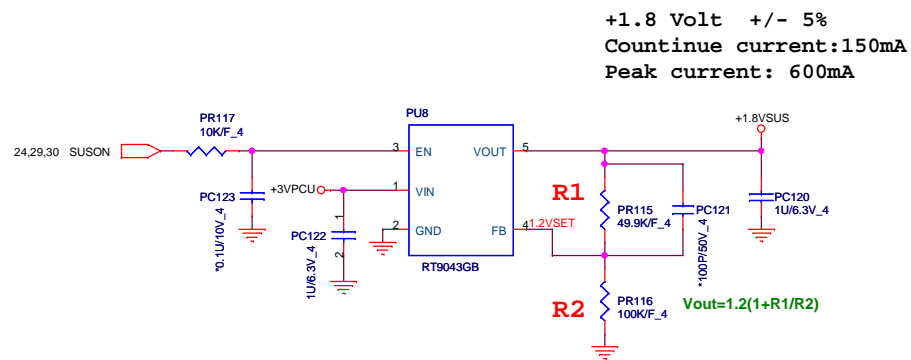
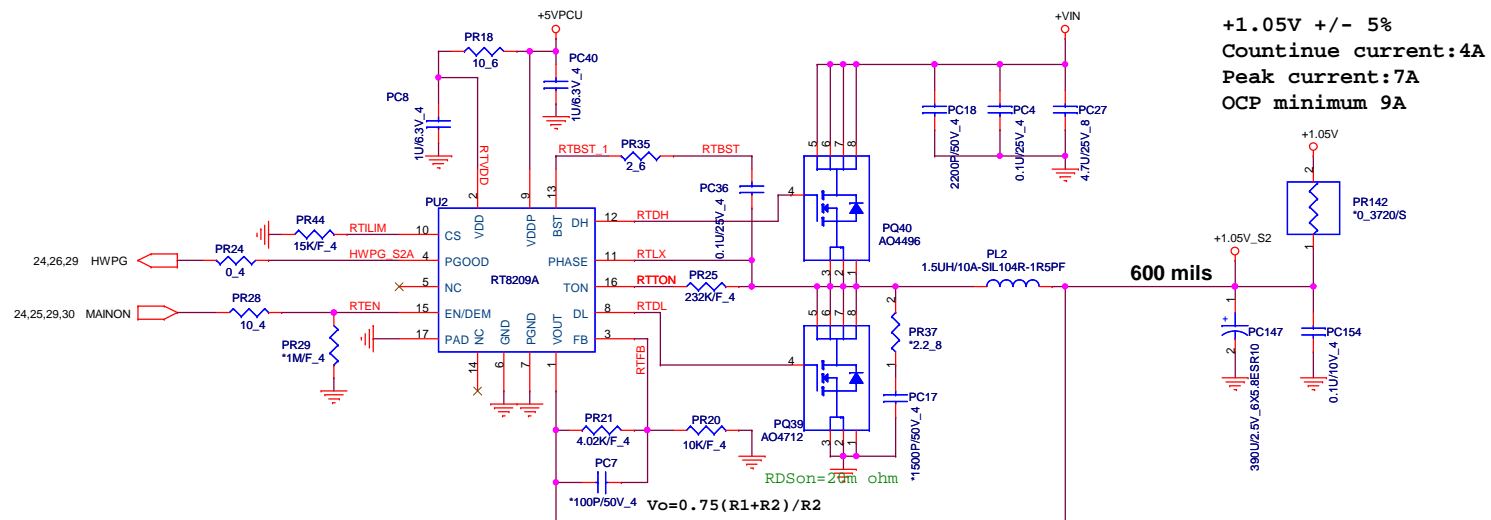
Place these CAPs
 close to FETs



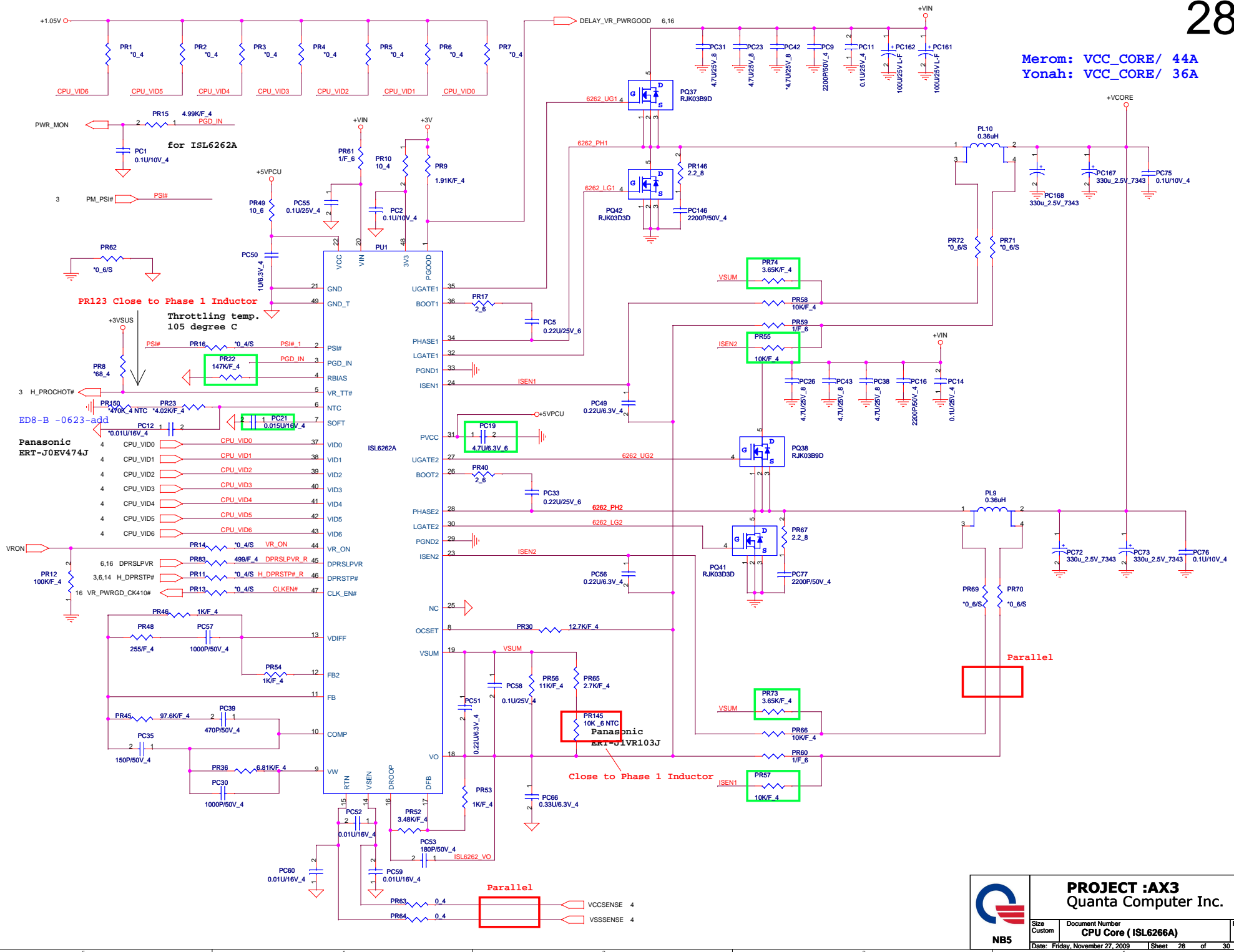
NTC need place under CPU Socket
 CPU Thermal protection at 90 +/-3 deგრrec




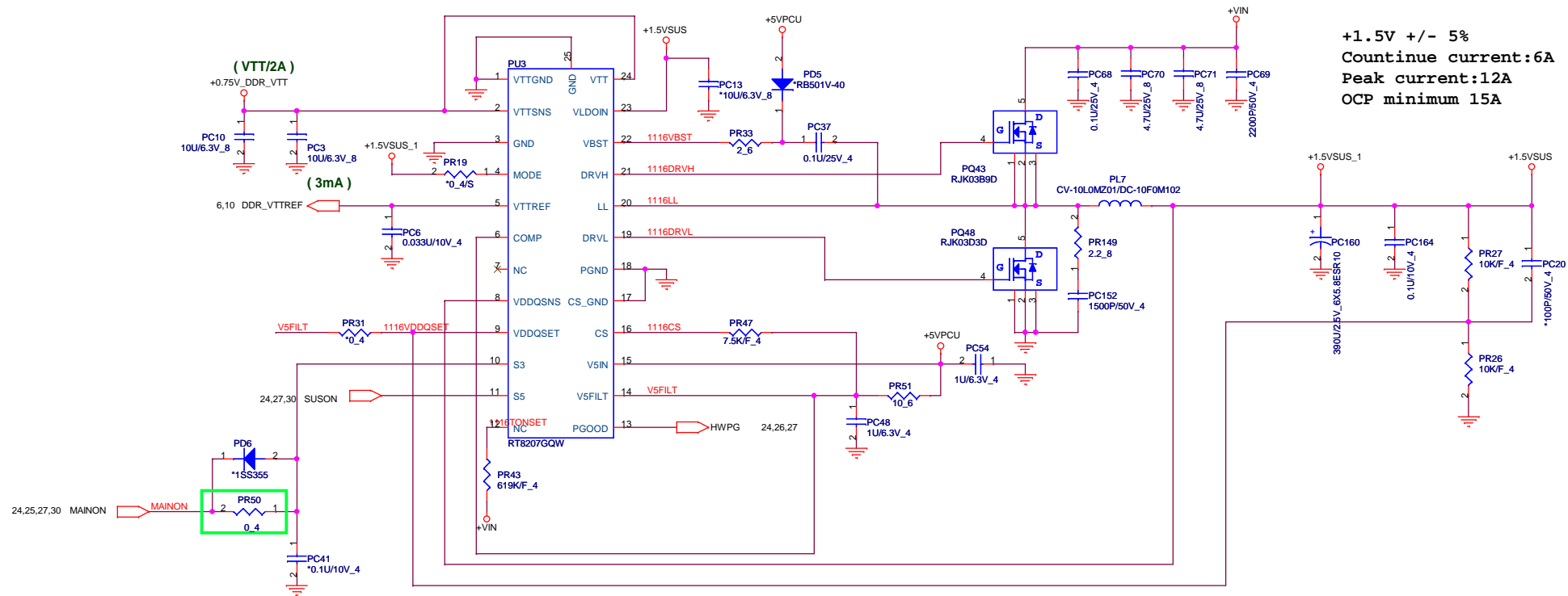
	PROJECT :AX3 Quanta Computer Inc.	
	Size Custom	Document Number +5V/+3V (RT8206B)
Date: Friday, November 27, 2009 Sheet 26 of 30		




Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A



	PROJECT :AX3	
	Quanta Core Inc.	
	Size Custom Document Number CPU Core (ISL6266A)	Rev PV
Date: Friday, November 27, 2009 Sheet 28 of 30		



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

 NBS	PROJECT :AX3 Quanta Computer Inc.	
	Size Custom Document Number DDR3 (RT8207)	Date: Friday, November 27, 2009

